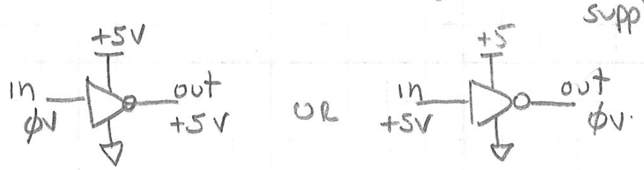
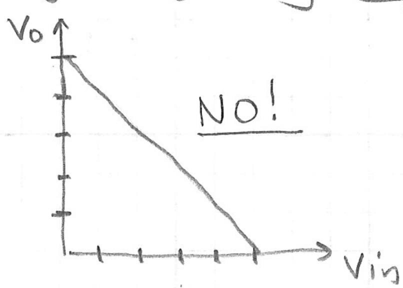
Digital Logic Inverter - An Analog/Digital Building Block

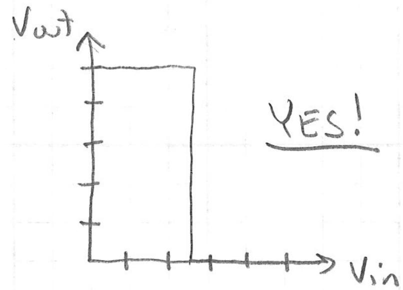
- symbol: 

- it "inverts" an input signal: ∅ volts input → supply voltage output
  supply voltage input → ∅ volts output

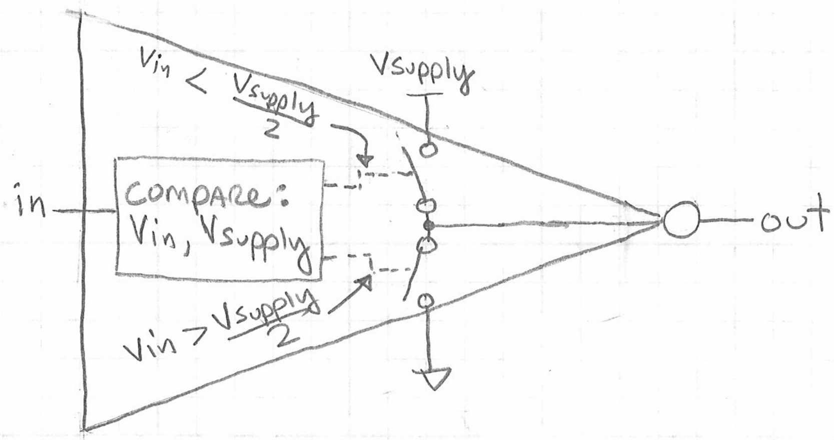


- the inversion is not linear; a decision is made at a threshold voltage, typically $\frac{V_{supply}}{2}$

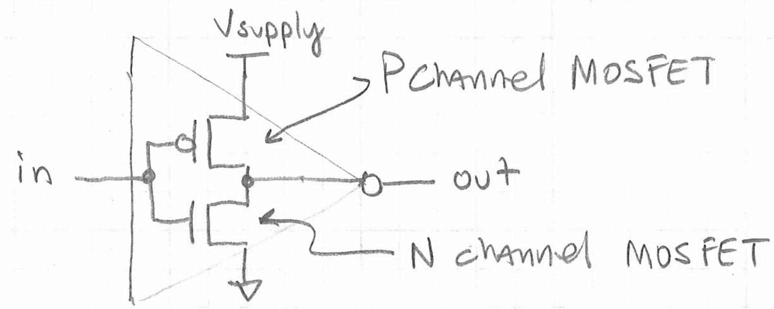




- The inversion is implemented by connecting the output to supply voltage or to ground via "switches"



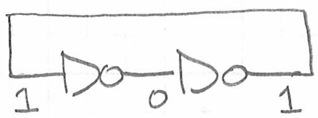
conceptually



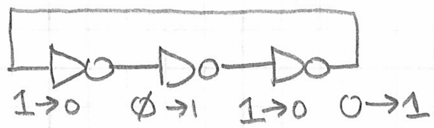
done with transistors

- In digital logic we speak of ∅ volts + Vsupply as "logic '∅'" and "logic '1'"
- "∅" + "1" may represent logical TRUE or FALSE or digits in a binary number
- In typical digital circuits, the power supply connections are not shown.

- What happens if we connect inverters together input to output?

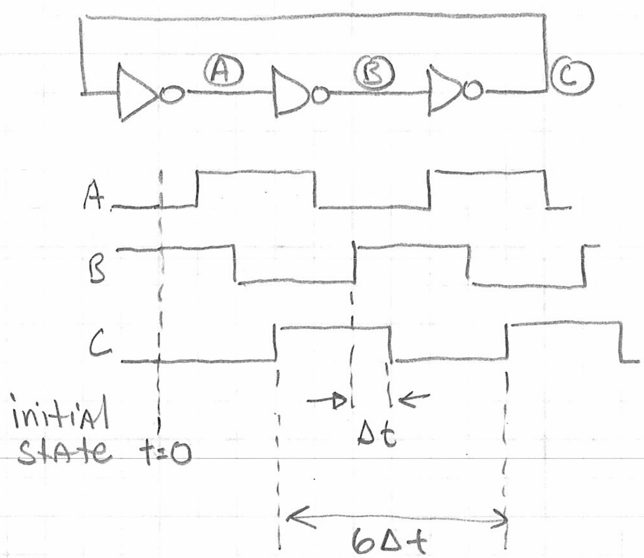


A steady state connection, holds a set value, → <u>memory cell</u>



An unstable condition, → <u>oscillator</u> (A ring oscillator)

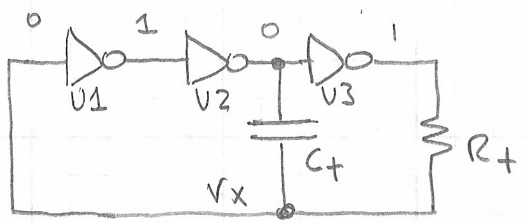
- The frequency of oscillation of the ring oscillator is determined by the delay of the signal through the inverters; the propagation delay



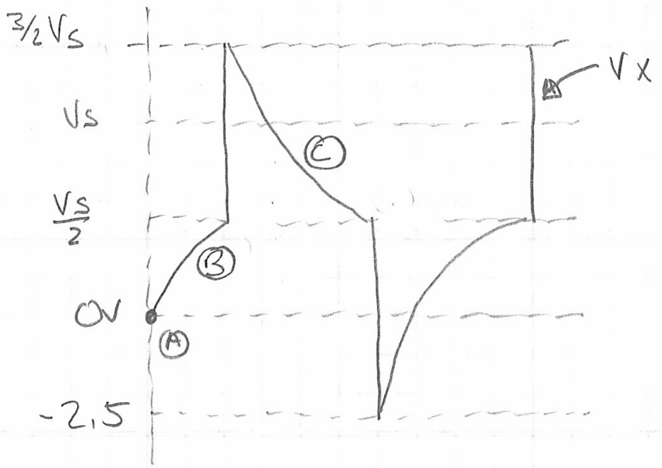
- Each inverter has a delay; Δt
- The 3 stage ring oscillator has a period of oscillation of $6\Delta t$
- Δt is typically about 5 ns (5×10^{-9} s)
- This oscillator would run at about 33 MHz. This is a shortwave radio frequency.

We can use the RC time constant to slow the ring oscillator down.

Consider this circuit:



- R_T + C_T will set the frequency of oscillation
- lets assume an initial condition and plot the voltage at Vx.



Ⓐ C_T is initially discharged @ 0V

Ⓑ C_T is charged by U3 till the threshold voltage $\left(\frac{V_s}{2}\right)$ is reached. At this point U1, U2, & U3 switch. This places the lower potential lead of C_T at Vs and its higher potential terminal at $\frac{3}{2}$ Vs

Ⓒ C_T is now discharged by U3 till it reaches $\left(-\frac{V_s}{2}\right)$ This plus the Vs output of U2 puts the input of U1 at the threshold again causing all inverters to switch again. This places Vx at $-\frac{V_s}{2}$ as U2's output is back at 0V,

Ⓓ C_T now charges again until it reaches the threshold again and the cycle repeats.