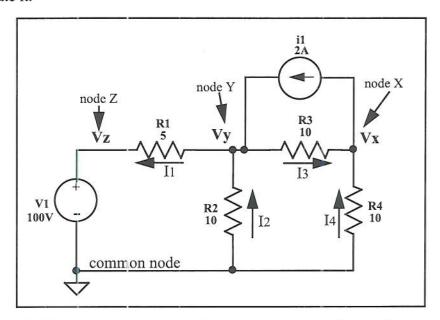
Using Spice for KCL Analysis

Below is a circuit analyzed by hand earlier. We shall now create a Spice netlist for this circuit and simulate it.

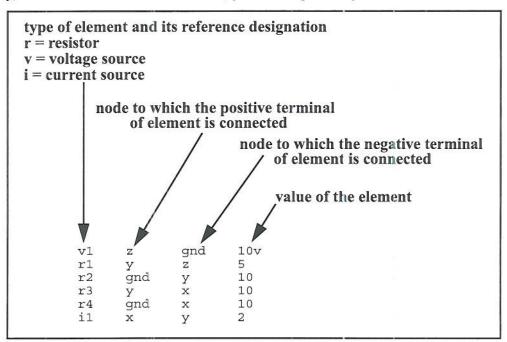


The Spice netlist for the circuit above is placed in a normal text file with whatever editor you like. It looks like this:

```
.title class example problem
   ** netlist follows *****
          gnd 10
v1
      z
r1
            z
r2
      gnd
            У
                10
      У
r3
                10
            x
                10
r4
      gnd
            x
                2
i1
      netlist done *****
.control
set numdgt=2
  op
  echo Node voltages:
 print line v(x) v(y) v(z) < note, this line chases to print out new notes.
  echo
  show v1 < sives into on V1
  quit
.endc
.end
```

The body of the netlist is shown below. A review of its format is given below. Note that nodes

Vx, Vy, and Vz have been abbreviated x, y and z respectively.



spice is invoked on the file kcl1.sp at the unix prompt by typing:

```
haspice kell.sp > output
```

The results from the simulation are in the file *output*:

```
** ngspice-21plus : Circuit level simulation program
** The U. C. Berkeley CAD Group
** Copyright 1985-1994, Regents of the University of California.
** Please submit bug-reports to: ngspice-bugs@lists.sourceforge.net
** Creation Date: Thu Jul 22 18:02:18 UTC 2010
Circuit: class example problem
                                     (kcl)
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
No. of Data Rows : 1
node voltages:
v(x) = -5.7e+00
v(y) = 8.57e + 00
v(z) = 1.00e+01
 Vsource: Independent voltage source
     device
                                  v1
         dc
                                  10
      acmag
      pulse
       sine
        sin
        exp
        pwl
       sffm
         am
           i
                          -0.285714
          p
                            2.85714
```

ngspice-21plus done