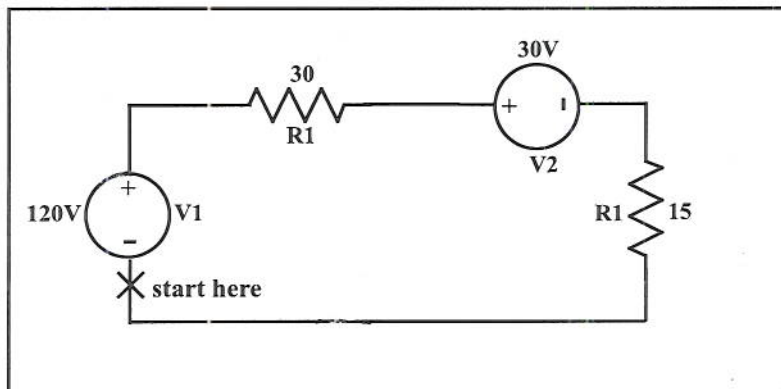


KVL Analysis with Spice

“Spice” or its derivatives (Spice 2G.6, Hspice, Pspice) are used to simulate the behavior of electrical circuits.

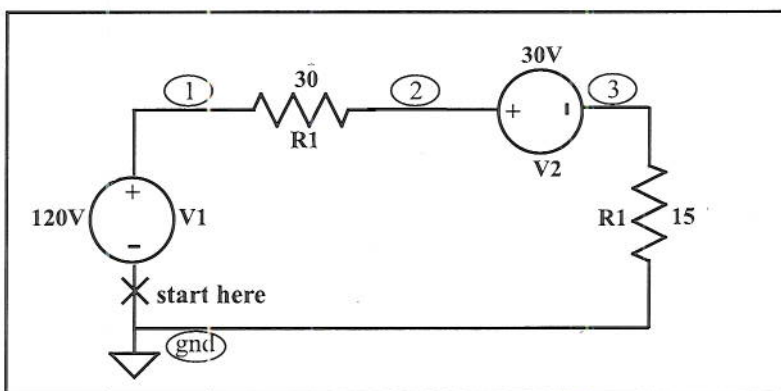
Using a circuit simulator is a good way of confirming your intuition about a circuit or confirming a hand analysis. It should basically be used as confirmation or optimization tool. It should not be used as a design tool. For this class, Hspice can serve as an easy and quick way to check almost any homework problem you can think of. Think of it as the ultimate answer key.

Below is the circuit we analyzed by hand earlier. We see that the steps of selecting a reference direction for the current I and element voltages have been done.



In Spice, circuits are described as “netlists”. Netlists are simply a listing of how the elements in the circuit are connected. We describe the connection of the elements by telling which node each terminal of an element is connected to. Therefore, we need to mark the nodes in the circuit with unique node names. These are shown below as the numbers 1,2,3 and the node name “gnd”. Note that all Spice netlists must have a ground node in the circuit. The node names are circled for clarity.

Each element in the netlist must be distinct from the others. Therefore, we need to distinguish the two voltage sources with reference designators. For this circuit, the designators are “V1” and “V2”. Note that R1 and R2 are already marked. The new annotated schematic is shown below. Now we can write the netlist.



The Spice netlist for the circuit above is placed in a normal text file with your choice of editor. It looks like this:

```
.title class example problem
```

```
***** netlist follows *****
v1 1 gnd 120
r1 1 2 30
r2 3 gnd 15
v2 2 3 30
***** netlist done *****
```

netlist

```
.control
set numdgt=2
op
echo Node voltages:
print line v(1) v(2) v(3)
echo
show R1
quit
.endc
```

simulator directives

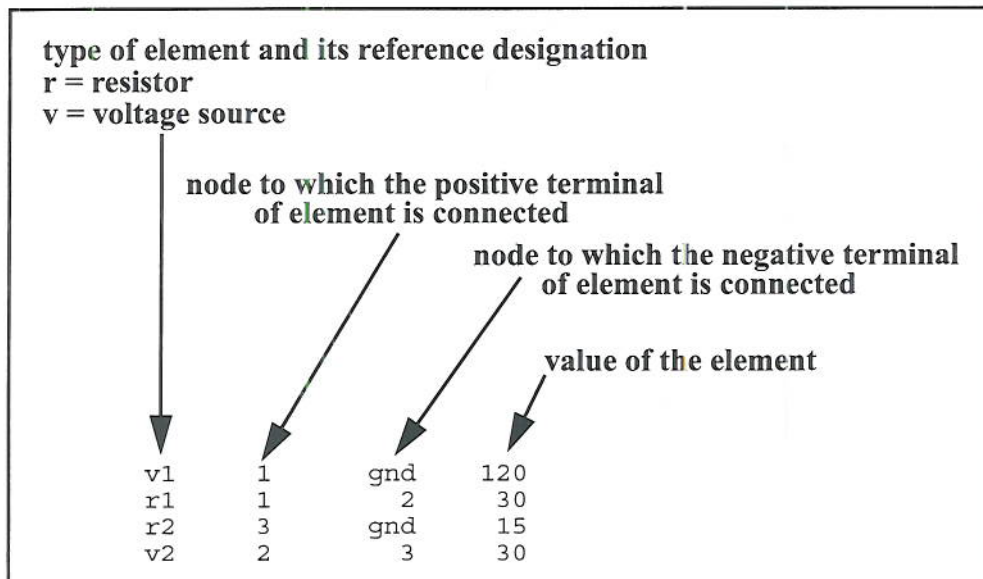
All in a text file
called Kvl.sp

```
.end
```

A description of the spice file is as follows:

The first line is always the title line. With or without the `.title`, the first line is still the title. (Watch out!)

The body of the netlist is shown below. It is the exact description of the circuit.



The `op` statement instructs Spice to run a dc steady state analysis.

The `.end` statement indicates the end of a Spice file. It is mandatory.

Comments follow the "\$" delimiter, or the "*"

Note that the currents through the elements in the netlist are implied by the positive and negative terminal definitions. Think about this.

If we name this file *kvl.sp*, *ngspice* is invoked on the file at the Unix prompt by typing:

ngspice kvl.sp > output

The results from the simulation are in the file *output*.

Circuit: class example problem

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

No. of Data Rows : 1

node voltages:

v(1) = 1.20e+02

v(2) = 6.00e+01

v(3) = 3.00e+01

Resistor: Simple linear resistor

device	r1
model	R
resistance	30
ac	30
dtemp	0
noisy	1
i	2
p	120

ngspice-21plus done

We see that the loop current is identical to the hand calculated value of 2A.

