The Tline Neighborhood

1. In figure 1, a fast CMOS buffer is driving a parallel terminated, 50Ω transmission line. The buffer is packaged in a high-performance QFN package. There is inductance in the PCB traces leading to the buffer chip \((L_{V_{dd}} = 100nH)\) as shown and there is no decoupling capacitor on the buffer \(V_{dd}\) pin.

![Figure 1: PCB with Inductive \(V_{dd}\) Trace](image1)

The waveforms for \(V_{dd}\) at the chip as well as the input and output of the transmission line are shown in figure 2. Two anomalous areas on the \(V_{dd}\) waveform are highlighted.

![Figure 2: PCB with Inductive \(V_{dd}\) Trace - Waveforms](image2)
(a) For each anomaly on $V_{dd}$, explain the root cause and mechanism. A good explanation would include the timing of the anomaly, shape of the waveform and its polarity. A thoughtful examination of the circuit will be necessary.

2. In figure 3 we see the previous circuit with an added decoupling capacitor connected to $Vdd\_pin$ of the buffer.

(a) Determine maximum allowed inductance for $L_{cap}$ that will keep $Vdd\_pin$ from varying more than $\pm10\%$. The decoupling capacitor is initially modeled as a ideal cap with a 5nh series inductance. Experiment with the netlist `decouple.sp` to find the correct value.

![Figure 3: Determine Allowed Decoupling Capacitor Inductance](image)

3. Refering to the schematic in figure 3, the following waveform is seen at $Vdd\_pin$ and the buffer output $tline\_in$ in figure 4. What choices for $L_{cap}$ and $C_{vdd}$ would cause these waveforms?

![Figure 4: What choice of $L_{cap}$ and $C_{vdd}$ would cause this?](image)
4. Suppose it is possible to insert a source terminating resistor between the output of the buffer and the transmission line, and remove the 50Ω load termination resistor as shown in figure 5.

![Diagram of decoupling capacitor with series-source termination](image)

**Figure 5: Decoupling Capacitor w/Series-Source Termination**

Experiment with the netlist `decouple_series.sp` to answer the following questions.

(a) Determine the correct value of the source terminating resistor $R_{\text{src}}$ for proper $V_{\text{dd}}$ switching at $\text{tline}_{\text{out}}$ and give the approximate output resistance of $\text{o_buffer}_\text{qfn}$.

(b) Determine minimum capacitance $C_{\text{vdd}}$ and maximum inductance $L_{\text{cap}}$ for the decoupling capacitor to allow signal at the near end of the transmission line to have less than 10% over or undershoot.

(c) For a given decoupling capacitor size, are there advantages to using the series terminated versus the parallel terminated connection? Explain your answer.

5. In the circuit of figure 5, suppose that the decoupling capacitor is of sufficient size for its purpose but that the internal inductance was too large to keep $V_{\text{dd}}_{\text{pin}}$ stable enough. What would be the effect of placing another identical capacitor in parallel with the first? What would you expect to see?

6. A CMOS digital driver with an output impedance of 12Ω drives a star network that consists of 8, equal length, branches that are each terminated with only a single CMOS inverter. The beginning of each branch starts directly at the driver output. What should the characteristic impedance of the lines be such that incident wave switching occurs at each receiver. In other words the incident wave results in a full $V_{\text{dd}}$-sized swing at the inverter inputs.

7. Sometimes a small inductor is placed at the output of a digital driver as shown in figure 6. What is the effect to the driving edge: Does it limit the voltage of the launched waveform, limit the current of the waveform or reduce overshoot?
8. A signal with slow edges or edges that transition slowly around the switching threshold often require a Schmitt-trigger receiver that has two distinct switching thresholds to prevent false triggering. Create a Schmitt-triggered buffer with two resistors R1 and R2 and a non-inverting CMOS buffer as shown in figure 7.

The non-inverting buffer operates from 3.3 volts. Its input threshold is 1.65 volts or \( \frac{V_{dd}}{2} \). The hysteresis is symmetrical around the switching threshold and is \( \pm 400 \text{mv} \). This gives the circuit a low-to-high threshold of 2.05 volts and a high-to-low threshold of 1.25 volts. The input impedance to the Schmitt trigger circuit must be \( 5K\Omega \). The buffer has an infinite input resistance and an zero output resistance. See figure 8 for threshold voltages.
9. Consider the two circuits in figure 9. Assume CMOS input receivers with very small but non-zero input leakage currents.

![Figure 9: Two different termination schemes](image)

(a) Determine the initial peak current caused by the incident wave as its launched into each transmission line. Which line requires a greater peak current to launch an incident wave?
(b) What is the DC steady-state current in each circuit.
(c) If the source terminating resistor in (a) had to be removed to reduce cost, and it was possible for you to set the size (width) of the N-channel driver transistor, what would its effective resistance be so no external termination resistor was needed?
(d) Suppose that instead of terminating the circuit in (b) with a parallel resistor, an attempt is made to terminate the far end of the circuit with a series resistor placed between the end of the transmission line and the input to the receiver as in figure 10. Would it work? Would it be effective? Why or why not?

![Figure 10: Series Termination to the Load](image)

(e) Suppose in the process of attempting to terminate a transmission line, an engineer determines that it is best to terminate the receiver end of the line as shown in figure 13.
What is obviously wrong with this circuit? Under what conditions might it "work"?

10. On some large IC packages, we see on-package decoupling capacitors as in figure 12.

Consider the partial schematic diagram below showing the power supply connection for one pin of a large IC. It shows both the bond wire inductance, the lead frame inductance and the pin inductance.

What portion of the inductance from the silicon die to the PCB power supply plane ($V_{dd}$) will the capacitor help negate? Why do you think the capacitors are located in the center of the
11. An engineer using an oscilloscope probes a source terminated transmission line at the far end before the receiving chip has been soldered in. The notes from his engineering notebook are reproduced below in figure 14. Later, the chip is soldered into the board. The chip is operating with a $V_{dd}$ of 3 volts. He records the waveform again at (b). What is the most likely cause for the improvement?

![Figure 14: Engineering Notebook Drawing Before and After Chip is Soldered In.](image)

12. What physical or practical limitations limit the upper and lower characteristic impedance:
   (a) on a PCB
   (b) of a coaxial cable
13. An engineer using an oscilloscope probes a three different source terminated transmission lines at their inputs. She sees the waveforms as shown below. In each case, state what the waveforms tell the engineer about the relative sizes of output driver impedance (in both high and low states), source termination resistor and the $Z_o$ of the transmission line. The supply voltage is 3.0 volts.

(a) Driver 1

(b) Driver 2

(c) Driver 3

(d) Driver 4
14. A source terminated transmission line is shown below in figure 16. The n-channel transistor is represented with a switch. Also shown are the parasitic inductances in both the PCB and the decoupling capacitor. Vdd is assumed to be 3.3 volts.

(a) Assume that $L_{pcb}$ is large and $L_{cap}$ is negligible. If $t_d = 2\,ns$, determine the size of decoupling capacitor required such that the node chip_vdd will experience less than 100mV of Vdd droop when a positive incident wave edge is launched.
(b) Is $t_d$ becomes 8ns, does the size of the capacitor change? Why or why not? (c) Suppose this circuit is changed so that the 50Ω source terminating resistor is shorted and a 50Ω parallel terminating resistor of is added at the end of the line. How will this effect the size required for the decoupling capacitor?

15. A properly executed parallel terminated transmission circuit is shown below in figure 17. The elements L and C represent discontinuities that are significant to circuit operation. Draw what the waveform would look like at the driver end tline_in of the circuit.

Figure 16: Decoupling Problem

Figure 17: Multiple Discontinuities on a Segmented Line