1. **Vdd Anomaly #1** is a sudden drop in Vdd supplied to the driver. This is due to the LVdd inductor limiting the current available to the driver. When the driver is current limited by the inductor, it cannot launch as big of an incident wave.

As time goes on, the current through the inductor begins to increase allowing the edge to eventually reach Vdd. The edge of the incident wave, however, follows Vdd-pin almost exactly as the inductor current increases.

Voltage at Vdd-pin droops because of the direction of current flow through the inductor. Vdd-Vdd-pin is a positive value which subtracts directly from the voltage supplied to the driver.

**Vdd Anomaly #2** is a result of the "inductive kick back" at the LVdd inductor. Near the end of the first pulse, the current has reached a steady state value through the inductor. The current sharply steady because of the parallel termination.

When the output buffer switches its output to a logic low state, almost no current is needed from Vdd. In a short period of time, the LVDD inductor sees a current change and produces a reverse polarity voltage in an attempt to maintain the previously flowing current. Remember that the inductor's nature is to oppose changes in current. We thus see a large positive spike in Vdd-pin.

(Note: Rising is evident in the simulation on Vdd. This is most likely due to resonant behavior between capacitance at Vdd-pin and the 100nH inductor.)