3. Referring to Figure 4, we can see that the inductive kickback at the falling edge of the first pulse is small. Also, the initial droop in V_{di,pin} is small at the rising edge of the pulse. These two clues indicate that the parasitic inductance of the decoupling capacitor is small.

Once the edge of the pulse is launched, the normally flat portion of the pulse begins and continues to droop. This is because the 50Ω parallel termination requires continuous current and the decoupling capacitor is of insufficient size to keep V_{di,pin} and thus time-in at a stable level.

We can also note that although the decoupling cap is connected to the PCB supply plane, its inductance is too large to keep the decoupling capacitor charged while the pulse is high. Between pulses, however, the capacitor gets enough charge to launch a second incident wave.