4. a) A source series resistor of about 45 ohms gives a \( V_{dd}/2 \) "shelf" on the rising and falling edges. Given that the Zo of the line is 50Ω, the Ro of the buffer is about 5Ω.

b) \( \pm 10\% \) of 3.3V is 3.63V ± 2.97 volts

One viable pair found was \( L_C \approx 0.5\)nH with \( C_{VDD} = 100\)nF. Decreasing \( C_{VDD} \) to 10nF still keeps the over & undershoot to < 1070.

c) For a fixed decoupling capacitance size, a series terminating line has advantages. First, the incident current launched into a T-line is less. Thus the capacitance has to supply less current to the driver and is able to keep \( V_{DD} \) more stable.

Since the incident current is less, the VDD capacitance can have more parasitic lead capacitance without causing problems. This may allow for a more relaxed capacitor placement or even a cheaper capacitor to be used.