Open-ended Design Problem

1. Consider the printed circuit board layout shown in fig [1]. Two drivers and five receivers are connected on a transmission line. Only one driver is on at any given time. Either driver, when enabled, should be able to correctly drive any of the loads on the board. The receiver inputs represent an input capacitance of 5pF with a switching threshold of $\frac{V_{dd}}{2}$. The drivers and receivers are powered from a Vdd supply of 3.3 volts at location "PS".

The characteristic impedance $Z_o$ of the signal "X" layer is 40 ohms and signal "Y" layer is 80 ohms. The power supply "X" layer exhibits a 40 ohm $Z_o$ and the "Y" layer a $Z_o$ of 50 ohms. Vias exhibit a capacitance of 2pF each for signal traces and an inductance of 1nH for power traces.

The board has a dielectric constant of $\epsilon_r$ of 4.5. You may route in a Manhattan grid (X and Y) only.

![Figure 1: Problem 1](image-url)
Your task is to create a network topology and termination scheme such that all the receivers see the driven signal from either driver within a 3nS window. This will also include a proper power supply distribution to the drivers and receivers. The waveform must also meet the following parameters.

(a) Rising edge overshoot will be less than +0.3V
(b) Falling edge undershoot will be less than -0.3V
(c) Rise(fall) time on both edges will be less than 3ns
(d) Delay between any receiver seeing the clock will be less than 3ns
(e) The switching threshold will be exceeded and held by at least 0.7 volts in either rising or falling case

Use the spice tar file located at: http://web.engr.oregonstate.edu/~traylor/ece391/new_hw/w2017/spice_files_w2017.tar
Do not change any of the models supplied for the drivers or receivers.

To turn in:
(a) Two voltage waveform plots indicating the driver and all receiving nodes. This plot should clearly show that all requirements (a-f) are met. Make the background to your plot white and not black. Plots that are unreadable or cannot be used to determine if the criterion are met will be given zero credit.
(b) Spice netlist of your circuit (printed with a2ps).
(c) A physical layout of your circuit.
(d) A schematic drawing of your circuit showing all values of components and transmission lines.
(e) An explanation as to your assumptions, approach and results. Keep this to less than one-half page.

• Metrics:
  – monotonic edges: 20%
  – overshoot: 10%
  – undershoot: 10%
  – risetime on edges: 10%
  – number of components used: 10%
  – Explanation of results: 40%