Heuristic Determination of T-line Environments
(not exact science..."it depends")

First look at the primarily digital environment.

Our question is answered by looking at:

"rise time" versus "flight time"

$t_r, t_f$ vs $t_d$

Flight time is the time it takes for the signal to traverse the signal path (one-way). We represent it as $t_d$. (Sometimes $t_f$) (confused with fall-time)

Rise Time (or Fall Time) $t_r$ or $t_f$

Note: For most CMOS circuits $t_r = t_f$ but not always.

normally measured at 10%, 90%
Heuristic Determination... (cont)

Wait a minute, what happened to frequency & wavelength?
Is there some relationship between rise, fall and frequency?
→ Yes!

Remember: Fourier Series Approximation for periodic square wave?

\[ f(x) = \frac{1}{2} + \sum_{k=1}^{\infty} \frac{2}{(2k-1)\pi} \sin((2k-1)x) \]

Ah yeah! A square wave is formed by summing an infinite number of
sine waves from the odd harmonics of a fundamental frequency, \( f, 3f, 5f \ldots \)

\[ f(x) = \frac{1}{2} + \frac{2}{\pi} \sin(x) + \frac{2}{3\pi} \sin(3x) + \frac{2}{5\pi} \sin(5x) \ldots \]

... So, sharp edged square waves contain very high frequency components,

... And edges with greater rise & fall have fewer high frequency components.

Rule of thumb: most energy is at frequencies below \( \frac{0.5}{\text{rise}} \) (Tektronix: \( \sim 0.35/\text{tv} \) for probes)
Rise - Time versus Flight Time

\[ t_d = \frac{l}{v_f} \]

To behave as a lumped circuit, the rise time of the driver must be slow enough such that a point on the edge is seen everywhere on the line at very nearly the same time.

This is congruent with our statement that lumped circuits "see" voltage or current changes simultaneously throughout the circuit.

A fast rising edge is equivalent to a rapid phase change.
Heuristic Determination...

- Digital Domain

Rise Time vs Flight Time

Compare the faster of \((\text{rise}, \text{fall})\) with the one way propagation delay through the signal path (aka "flight time")

\[
\text{delay} = \frac{\text{length of path}}{V_p}
\]

For CMOS IC's (and most others)

- If \(\text{rise} > 6 \times \text{delay}\); lumped circuit
- If \(\text{rise} < 2.5 \times \text{delay}\); not lumped circuit (T-line scenario)

In between those values, it depends.
- Data or clock signal
- Variation of temperature, voltage, process variations

Flip-flop clock inputs must be monotonic. The "D" input is far more forgiving.
### Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( V_{CC} )</th>
<th>MIN</th>
<th>TYP(1)</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OH} )</td>
<td>( I_{OH} = -100 , \mu A )</td>
<td>0.8 V to 2.7 V</td>
<td>( V_{CC} - 0.1 )</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>( I_{OH} = -0.7 , mA )</td>
<td>0.8 V</td>
<td>0.55</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( I_{OH} = -3 , mA )</td>
<td>1.1 V</td>
<td>0.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( I_{OH} = -5 , mA )</td>
<td>1.4 V</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( I_{OH} = -8 , mA )</td>
<td>1.65 V</td>
<td>1.2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( I_{OH} = -9 , mA )</td>
<td>2.3 V</td>
<td>1.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>( I_{OL} = 100 , \mu A )</td>
<td>0.8 V to 2.7 V</td>
<td>0.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>( I_{OL} = 0.7 , mA )</td>
<td>0.8 V</td>
<td>0.25</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( I_{OL} = 3 , mA )</td>
<td>1.1 V</td>
<td>0.3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( I_{OL} = 5 , mA )</td>
<td>1.4 V</td>
<td>0.4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( I_{OL} = 8 , mA )</td>
<td>1.65 V</td>
<td>0.45</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( I_{OL} = 9 , mA )</td>
<td>2.3 V</td>
<td>0.6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{I} )</td>
<td>( I_{I} = ) A inputs</td>
<td>( V_I = V_{CC} ) or GND</td>
<td>0 to 2.7 V</td>
<td>±0.5</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>( I_{off} )</td>
<td>( V_I ) or ( V_O = 2.7 , V )</td>
<td>0</td>
<td></td>
<td></td>
<td>±10</td>
<td>µA</td>
</tr>
<tr>
<td>( I_{CC} )</td>
<td>( V_I = V_{CC} ) or GND</td>
<td>( I_O = 0 )</td>
<td>0.8 V to 2.7 V</td>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>( C_I )</td>
<td>( V_I = V_{CC} ) or GND</td>
<td>2.5 V</td>
<td>2.5</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

(1) All typical values are at \( T_A = 25^\circ C \).

### Switching Characteristics

over recommended operating free-air temperature range, \( C_I = 15 \, pF \) (unless otherwise noted) (see Figure 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>( V_{CC} = 0.8 , V )</th>
<th>( V_{CC} = 1.2 , V )</th>
<th>( V_{CC} = 1.5 , V )</th>
<th>( V_{CC} = 1.8 , V )</th>
<th>( V_{CC} = 2.5 , V )</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>TYP</td>
<td>MIN</td>
<td>MAX</td>
<td>TYP</td>
<td>MIN</td>
<td>MAX</td>
</tr>
<tr>
<td>( t_{pd} )</td>
<td>A</td>
<td>Y</td>
<td>4.8</td>
<td>0.7</td>
<td>3.3</td>
<td>0.5</td>
<td>2.9</td>
<td>0.5</td>
</tr>
</tbody>
</table>

### Switching Characteristics

over recommended operating free-air temperature range, \( C_I = 30 \, pF \) (unless otherwise noted) (see Figure 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>( V_{CC} = 1.8 , V )</th>
<th>( V_{CC} = 2.5 , V )</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{CC} ) = 0.15 , V</td>
<td>( V_{CC} ) = 0.2 , V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
</tr>
<tr>
<td>( t_{pd} )</td>
<td>A</td>
<td>Y</td>
<td>0.6</td>
<td>1.4</td>
<td>2.5</td>
</tr>
</tbody>
</table>

### Operating Characteristics

\( T_A = 25^\circ C \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( V_{CC} = 0.8 , V )</th>
<th>( V_{CC} = 1.2 , V )</th>
<th>( V_{CC} = 1.5 , V )</th>
<th>( V_{CC} = 1.8 , V )</th>
<th>( V_{CC} = 2.5 , V )</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_{pd} )</td>
<td>Power dissipation capacitance</td>
<td>16</td>
<td>17</td>
<td>17</td>
<td>17</td>
<td>19</td>
<td>pF</td>
</tr>
</tbody>
</table>
Most CMOS ICs exhibit $t_r + t_f = 1.0 - 2.5\, \text{nS}$. (AC, UHC families) (< 1\, \mu\text{m})

Typical PCB is FR-4 fiberglass with velocity of prop. $= 0.45\, \text{c}$

Remember that $V_p = \frac{c}{\sqrt{\epsilon_r}}$; FR-4 $\epsilon_r = 4.7$ (FR-4: Fire Resistant, fiberglass; epoxy laminate).

Example: How long can the interconnect be at the output of a 7440Q04 when placed on a PCB with $V_p = 0.45\, \text{c}$ and be confidently treated as a lumped element?

Shooting for $\frac{t_r}{t_{\text{delay}}} \geq 6$; so

$$\frac{0.5 \times 10^{-9} \, \text{s}}{0.45 \, \text{m/s}} > 6$$

$$\frac{\Delta L}{0.45 \, \text{c/m/s}}$$

$$\left(0.5 \times 10^{-9} \, \text{s}\right) 0.45 \left(300 \times 10^6 \right)^{\frac{2}{3}} > 6$$

$$\Delta L = \left(0.5 \times 10^{-9} \, \text{s}\right) 0.45 \left(300 \times 10^6 \right)^{\frac{2}{3}} \left(\frac{1}{6}\right)$$

$$L = 11.25\, \text{mm} = 0.4\, \text{"} \quad \text{(Confidently lumped)}$$

If $\frac{t_r}{t_f} > 2.5$ ....

$$L = 27\, \text{mm} = 1.0\,\text{"} \quad \text{(Better be careful)}$$
Heuristic Determination...

Slower CMOS parts (μCs) can typically drive ~6" traces or wires without problems.

Given standard FR-4 PCBs, a quick judgement can usually be made by knowing the logic family, the length of the trace and the topology of the trace.

* Note that the proceeding rules of thumb only work for point-to-point connections with proper drivers receivers & possibly terminations.

pt. to point:   \[\text{Do} \rightarrow \text{Do}\]

not! point to point: \[\text{Do} \rightarrow \text{Do} \rightarrow \text{this can be a blem} \rightarrow \text{to make work!}\]

What would the impact be if we simply treated all interconnect as if it was a transmission line?
Be careful with assumptions of $\tau = tf$. They vary with $VDD$, temperature, and vendor lot. 2:1 variations are possible. "When in doubt, scope it out."

Flight time on a PCB is dependent on $Er$ (typ 4.7) and the layer the trace is on. $\tau_p = \frac{L}{V_p}$

- $Er = 4.7$
- $VDD$ plane

- $Er = 4.7$
- Signal traces

$VSS$ plane

- All of E-field is contained within the $Er$ of the board. (Slower traces)

- Part of E-field is in the P2-4. $Er = 4.7$. Part of E-field is in air. Effective $Er$ is somewhat different and is lower. (Faster traces)

To summarize, "T-line or not" in the digital environment depends on:

- Rise/fall time of the driver
- Velocity of propagation of the medium
- Physical length of the medium

"Electrical length" (A time or phase angle)
Signal tr as a function of $t_d$ (flight time)

0$+t_d$

2.5$+t_d$

6$+t_d$

- **Time-critical** sgs or edge-sensitve sigs first $tr/4f$
  - (clock, reset...)

- **Non-critical** sgs data with $tsw > 6+t_d$

<table>
<thead>
<tr>
<th>SIMULATE &amp; CHECK AFTER LAYOUT</th>
<th>NO WORRIES</th>
</tr>
</thead>
</table>

  | SIMULATE & CHECK AFTER LAYOUT | CONSIDER QUICK HAND ANALYSIS | NO WORRIES |