The Lattice (or Reflection) Diagram

The lattice diagram provides a graphical bookkeeping method to keep track of reflections from both near and far ends of a T-line.

It can also be used when multiple T-lines of different Zo are in series.

It shows the impedance boundaries:

- Reflection coefficients at each end
- Flight time
- Voltage and current at any point (z = c't) on the line
- Cumulative voltage at both ends of the line

A voltage or current waveform versus time plot can be made from the lattice diagram.
The Lattice Diagram

Source Reflection Coefficient

\[ P_s = \frac{R_{sec} - Z_0}{R_{sec} + Z_0} \]

Load Reflection Coefficient

\[ P_L = \frac{R_L - Z_0}{R_L + Z_0} \]

\[ V_{sec} \left( \frac{Z_0}{Z_0 + R_{sec}} \right) = V_1^+ \]

\[ V_1^+ + P_L V_1^+ = V_1^+ \left( 1 + P_L \right) \]

\[ V_2^+ + P_L V_2^+ + P_L P_L V_1^+ = V_2^+ \left( 1 + P_L + P_L^2 \right) \]

\[ V_3^+ + P_L V_3^+ + P_L P_L V_2^+ + P_L P_L^2 V_1^+ = V_3^+ \left( 1 + P_L + P_L P_L + P_L^2 \right) \]

The eventual cumulative voltage at each end of the T-Line converges to:

\[ V_\infty = V_{sec} \left( \frac{R_L}{R_L + R_S} \right) \]
Lattice Diagram - single driver/receiver, source termination too big

\( P_s = \frac{75 - 50}{75 + 50} = 0.2 \)  \( P_L = \frac{\infty - 75}{\infty + 75} = 0.2 \)

\( V_{d^+} = 1 \cdot \left( \frac{50}{50 + 75} \right) = 0.4 \)

\( V_{d^-} = \frac{4 + 4 + (2 \times 4)}{4} = 0.88 \)

\( 4 \text{ ns} \)

\( 0.88 + 0.8 + (2 \times 0.8) = 0.976 \)

\( 5 \text{ ns} \)

Source termination is too big!

Excessive delay

Volts

0.0

0.4

0.8

1.0

\( 976 \text{ ns} \)

\( 96 \text{ ns} \)

\( 0 \text{ to } 5 \text{ ns} \)
Lattice Diagram - Single Driver/Receiver, Source Terminination too small

\[ Z_0 = 50 \Omega \]

openckt (-Do)

74AC1240 equivalent to:

\[ SV \pm 14 L \]

(\( \frac{p}{} \), \( \frac{p}{0} \), \( \frac{p}{0} \)) (Assumption if \( t_{del}=0 \))

\[ (p<0, \ p>0) \]

equipment ckt:

\[ V_1^+ = 5 \left( \frac{50}{14+50} \right) = 3.91 \text{V} \]

\[ V^+ = 3.91 + 3.91 + (-0.56 \times 3.91) = 5.63 \]

\[ V = 5.63 - 2.19 + (-0.56 \times -2.19) = 4.66 \]

\[ V = 4.66 + 1.23 + (-0.56 \times 1.23) = 5.2 \text{V} \]

\[ V = 5.2 - 0.69 + (-0.56 \times -0.69) = 4.9 \text{V} \]

\[ V_{\text{load}} = 7.82 \]

\[ 5.9 \]

\[ 4.5 \]

\[ 3.44 \]

\[ 2 \]

\[ 1 \]

\[ 0 \]

\( t=0 \)

\( t_d = 1 \text{ns} \)

\( t=1 \text{ns} \)

\( t=3 \text{ns} \)

\( t=4 \text{ns} \)

\( t=6 \text{ns} \)

\( t=8 \text{ns} \)

\( t=10 \text{ns} \)

\( V_{\text{load}} \)

\( V \text{ gate oxide, ESD damage} \)

Converging on 5V in steady state