The T-Line Neighborhood - Power Supply

The power supply connection must be considered as part of the signal chain for digital ICs.

When the P-channel transistor turns on - it connects VDD to the output pin. N-channel "" "" VSS to the output pin.

If VDD or VSS are ""dirty"" or they cannot support the current required, it will be apparent on the output pin.

The electrolytic capacitor at the regulator provides ""bulk"" decoupling and ""pole setting for the voltage regulator. It is usually physically & electrically far away to provide current rapidly to the IC.
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"Decoupling" capacitors decouple the IC from the inductance leading to the low impedance power source. It does so by providing a fast, local source of current to launch edges and support internal operation of the IC.

VDD or VSS traces can be long enough to present its T-Lines to power pins. A 0.125" trace on a 0.062" board is about 50Ω. This is an extremely wide trace. Would you want to power your IC's through a 50Ω resistor?!

For decoupling capacitors to be effective, inductance to the capacitor must be minimized. This is done by using physically small capacitors and short leads. SMD chip caps or ceramic disk caps are best.

Capacitor internal or lead inductance is part of equation put physical placement is also critical.
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IC packages that have power pins on the package corners are the worst performers.

![Diagram of loop with text: In a coiled wire, the larger the loop, the greater the inductance. The complete loop must be considered, VDD to cap to VSS.]

A much better solution would be a SMD cap on the bottom side of the board. The loop area is greatly reduced.

![Diagram showing SMD cap on the bottom side of a board]

An extreme solution was TI's AC11000 family with "Center VDD VSS" pins.

2 VSS pins in center → 2 VDD pins in center

![Diagram of AC11000's pinout with text: 'AC11000, 'ACT11000 QUADRUPLE 2-INPUT POSITIVE-NAND GATES (TOP VIEW) 1A 1 16 1B 1Y 2 15 2A 2Y 3 14 2B GND 4 13 VCC GND 5 12 VCC 3Y 6 11 3A 4Y 7 10 3B 4B 8 9 4A]

2 SMD caps could be placed directly underneath the package VDD + VSS pins. Technically excellent, a failure in the marketplace.
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If braided decoupling capacitors are used, lead length must be minimized.

Imagine:

\[ V_{dd} = 3.3V \]

0.1 \( \mu \)F cap, each lead 0.5", leads have dia of 0.01".

\[ L = \frac{5.08}{d} \left[ \ln \left( \frac{d}{2} \right) - 1 \right] \quad \text{where} \quad L = \text{length}, \ d = \text{dia in inches}, \ L \text{ in nH} \]

\[ = \frac{5.08(1)}{2} \left[ \ln \left( \frac{0.01}{2} \right) - 1 \right] \quad (1" \text{ total length}) \]

\[ = 25 \text{nH} \]

\[ V_L = \frac{dL}{dt} \quad \text{let's compute the effect of lead inductance} \]

\[ \frac{di}{dt} = \frac{3.3}{50} \quad \text{going from 0 to 3.3V into } 50\Omega \text{ line} \]

\[ \frac{V_L}{2nS} \quad \text{it does so over about } 2nS \]

\[ V_L = \left( 25 \times 10^{-9} \right) \left( \frac{70 \times 10^{-3}}{2 \times 10^{-9}} \right) = 0.88V \]
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What if we terminated at the source? Is this better? Any advantage?

AC04 Pout = 15J

Now,

\[
\frac{dI}{dt} = \frac{3.3}{2 \times 10^{-3}} \quad \{\text{series, source termination is easier to drive!}\}
\]

\[
V_L = (25 \times 10^{-9}) \left( \frac{40 \times 10^{-3}}{2 \times 10^{-3}} \right) = 0.5V \quad \{\text{much better, but pretty nasty! shorten the lines!}\}
\]

So, where and how we provide termination, can make a big difference in performance.
The impedance of a 0.1μF ceramic capacitor with 0.5" leads:

At resonance: \( F = \frac{1}{2\pi \sqrt{LC}} \)

For 0.1μF cap, 0.5" leads

Resonates at 2.7 MHz, beyond this freq, it's looking more and more like an inductor from a cap.

Note higher self-resonant frequencies of ceramic SMD caps

0805 package

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