Termination Strategies

- **Source [Series] Termination**
  \[ R_t = R_{out} - Z_0 \]
  - Only one extra component
  - Adds no DC load
  - Lower instantaneous current requirements
  - Less cross talk induced

- **Parallel [Load and J] Termination**
  \[ R_t = Z_0 \]
  - Slower edge rate due to DC loading
  - Can terminate to Vcc or Vss (flexibility)
  - Can be used with open drain drivers
  - \( R_t \) is easy to determine (only \( Z_0 \) dependent)
  - Only one component
  - DC power is dissipated in \( R_t \)
  - Needs decoupling if terminating to Vcc

- **Thevenin Termination**
  \[ R_{t1} || R_{t2} = Z_0 \]
  - Less DC load than simple parallel termination
  - Must take care with DC levels to avoid
    linear operation of CMOS receivers (tri-state bus)
  - \( R_t + R_{t2} \) can be chosen to "help"
    unbalanced \( R_{out} \) output buffers
  - Slower edge rate due to DC load
  - Usually seen on older TTL ckt's
Termination Strategies

- AC termination

A number of equations exist for determining $C_t$. These form a good starting point only. Basically, select $C_t$ big enough to terminate the edge. Typical values are $\times 50 - 100 \mu F$.

$R_t = Z_0$

+ Behaves much like parallel method
+ $R_t$ chosen $= Z_0$
+ $C_t$ can be difficult to optimise
+ No DC power dissipation
+ Full noise margins available
+ Can lead to timing problems
+ Good for clock signals
- Data pattern dependent delays

- Diode Termination

$V_{DD}$

$Z_0$

$\hat{X}$

Schottky diodes

+ Don't need to know $Z_0$
+ Diodes can be placed anywhere reflections are present.
+ Need to use fast, low Vf diodes
+ Not really a matching or termination strategy