The T-Line Neighborhood

Transmission lines do not operate in a vacuum. Ideally, they are a perfect conduit of the signals we place on them.

A T-Line at best can only pass the signal its given. That signal must be as electrically clean as possible, be launched properly, and be received properly.

The T-Line neighborhood could be viewed like this:

![Diagram of T-Line neighborhood]

Let's explore drivers & receivers first and develop some models for them that are useful to use in everyday work.
The T-Line Neighborhood - Driver and Receiver Models

We have used some very simple models for our digital drivers. For many applications they are totally adequate.

We can develop good first order driver and receiver models from:
- Spice model files
- V/I characteristics
- Direct observation

* Spice model of CMOS ICs . . . no way! Family jewels are there.
  Instead: IBIS (I/O Buffer Information Specification)
  - Intel 1993
  - Accurate, > 90% of spice I/V tables + timing info
  - IP protected
  - Much faster simulation (25x)
  - Bundled with PCB tools ($$$ $$$)
  - Spice Files Available only via NDA

A 'smutized' technology file
from a company I've been asked to not mention.
The T-Line Neighborhood - Driver and Receiver Models

Some companies will supply V/I characteristics for their parts. Estimates of driver output resistance can be inferred. These are usually typical values, not guaranteed.

- **V/I characteristics**
  - For AC CMOS family: Fairchild Semi Document M$Q10158$
  - Lists V/I characteristics of output buffer
  - For AC$Q$ output driven fig 7, 9 on pg 5

![Diagram 1](image1)

![Diagram 2](image2)

\[
R_{out(\text{low})} = \frac{\Delta V}{\Delta I} = \frac{1.5 - 0}{150 \, mA} = 10 \, \Omega \\
R_{out(\text{high})} = \frac{\Delta V}{\Delta I} = \frac{5.5 - 2.2}{150 \, mA} = 22 \, \Omega
\]

To calculate a single termination resistor for source termination, we can simply average \( R_{out} \) to arrive at an average \( R_{out} \) of \( \approx 16 \, \Omega \).
The T-Line Neighborhood - Driver + Receiver Models

When no other data can be found, direct measurement and observation can reveal a wealth of information about drivers + receivers.

- **Direct Observation**
  - **DC measurement**
    - Determine $V_{DS}$?

- **Test circuit to measure $V_{DS}$ when output is high.**
  - Adjust $R_X$ until output pin = $V_{DD}/2$
  - At that point, $R_X \approx V_{DS}$
    - (Basic test)
    - (Sourcing 120mA e)
    - (3.3V, output)

- **AC measurement**
  - Most accurate (if you can do it)

- Choose $Z_0$ to closely represent the eventual line to be driven. Find $R_X$ such that $V_{IN}$ entering into line is $V_{DD}/2$.
  - Then $V_{DS} = Z_0 = R_X$

This test will also reveal rise & fall times.

First step should be $V_{DD}/2$.
The IT-Line Neighbourhood - Driver + Receiver Models

The IV characteristics of a typical CMOS receiver are relatively simple. To the 1st order, it presents as a small value capacitor, perhaps 2-5pF.

It's a little more complex than that, however. It has an input protection structure that can be modeled as a pair of diodes between VDD and VSS.

ESD diodes are for static protection.

They are very small, fast, and are intended for only a few static strikes. (tv 0.7-1ns)

They are not intended as termination structures.

In normal operation, the ESD diodes should never be on. However, if severe over or undershoot occur, they will attempt to divert the energy of the waveform into the power supply.

How much current could a 3V overshoot inject into the on-chip power rail with VDD = 5V and Zo = 50Ω? What is the model?
The T-Line Neighborhood - Driver & Receiver Models

\[
\frac{8.5 - 0.6}{150} = 16 \text{mA}
\]

2.4V dropped by ZO + R thus gates experience 5.6V peaks. This is a reliability issue.

3V overshoot, 50Ω, 5V system

74AC00, 74ACT00 — Quad 2-Input NAND Gate

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC} )</td>
<td>Supply Voltage</td>
<td>-0.5V to +7.0V</td>
</tr>
<tr>
<td>( I_{LK} )</td>
<td>DC Input Diode Current</td>
<td>( V_I = -0.5 ) ( V_I = V_{CC} + 0.5 ) ( -20 \text{mA} ) ( +20 \text{mA} )</td>
</tr>
<tr>
<td>( V_I )</td>
<td>DC Input Voltage</td>
<td>-0.5V to ( V_{CC} + 0.5 )</td>
</tr>
<tr>
<td>( I_{OK} )</td>
<td>DC Output Diode Current</td>
<td>( V_O = -0.5 ) ( V_O = V_{CC} + 0.5 ) ( -20 \text{mA} ) ( +20 \text{mA} )</td>
</tr>
<tr>
<td>( V_O )</td>
<td>DC Output Voltage</td>
<td>-0.5V to ( V_{CC} + 0.5 )</td>
</tr>
<tr>
<td>( I_O )</td>
<td>DC Output Source or Sink Current</td>
<td>( \pm 50 \text{mA} )</td>
</tr>
<tr>
<td>( I_{CC} ) or ( I_{GND} )</td>
<td>DC ( V_{CC} ) or Ground Current per Output Pin</td>
<td>( \pm 50 \text{mA} )</td>
</tr>
<tr>
<td>( T_{STG} )</td>
<td>Storage Temperature</td>
<td>(-65^\circ \text{C to } +150^\circ \text{C})</td>
</tr>
<tr>
<td>( T_J )</td>
<td>Junction Temperature</td>
<td>140°C</td>
</tr>
</tbody>
</table>
The T-Line Neighborhood - Packaging

IC drivers & receivers do not live in a vacuum either. They are enclosed within a package which represents a very complex network that affects the quality of the signal strongly.

Package parasitics are available from manufacturers. Packages are not "rocket science".

Simply put, package size is the best predictor of parasitic LCRR magnitudes.

<table>
<thead>
<tr>
<th>Attribute</th>
<th>SOIC-14 (D)</th>
<th>SSOP-14 (DB)</th>
<th>TSSOP-14 (PW)</th>
<th>TVSOP-14 (DGV)</th>
<th>QFN-14 (RGY)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length, mm</td>
<td>8.65 ±0.10</td>
<td>6.20 ±0.30</td>
<td>5.00 ±0.10</td>
<td>3.60 ±0.10</td>
<td>3.50 ±0.15</td>
</tr>
<tr>
<td>Width, mm</td>
<td>6.00 ±0.20</td>
<td>7.80 ±0.40</td>
<td>6.40 ±0.20</td>
<td>6.40 ±0.20</td>
<td>3.50 ±0.15</td>
</tr>
<tr>
<td>Height, Max., mm</td>
<td>1.75</td>
<td>2.00</td>
<td>1.20</td>
<td>1.20</td>
<td>1.00</td>
</tr>
<tr>
<td>Pitch, mm</td>
<td>1.27</td>
<td>0.65</td>
<td>0.65</td>
<td>0.40</td>
<td>0.50</td>
</tr>
<tr>
<td>Footprint, mm²</td>
<td>51.90</td>
<td>48.36</td>
<td>32.00</td>
<td>23.04</td>
<td>12.25</td>
</tr>
<tr>
<td>Weight, g</td>
<td>0.127</td>
<td>0.122</td>
<td>0.056</td>
<td>0.040</td>
<td>0.032</td>
</tr>
<tr>
<td>Area savings, %</td>
<td>76.40</td>
<td>74.67</td>
<td>61.72</td>
<td>46.83</td>
<td>-</td>
</tr>
</tbody>
</table>

14-Pin QFN Comparison to Alternative Package Solutions

SOIC, 14 pin

<table>
<thead>
<tr>
<th>Pin</th>
<th>Rpk6</th>
<th>Lpk6</th>
<th>Cpk6</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.033</td>
<td>3.9nH</td>
<td>0.62pF</td>
</tr>
<tr>
<td>7</td>
<td>0.034</td>
<td>3.9nH</td>
<td>0.63pF</td>
</tr>
<tr>
<td>8</td>
<td>0.034</td>
<td>3.9nH</td>
<td>0.63pF</td>
</tr>
<tr>
<td>14</td>
<td>0.033</td>
<td>3.9nH</td>
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QFN, 14 pin

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<th>Lpk6</th>
<th>Cpk6</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.035</td>
<td>0.78nH</td>
<td>0.3pF</td>
</tr>
<tr>
<td>7</td>
<td>0.032</td>
<td>0.71nH</td>
<td>0.32pF</td>
</tr>
<tr>
<td>8</td>
<td>0.035</td>
<td>0.78nH</td>
<td>0.31pF</td>
</tr>
<tr>
<td>14</td>
<td>0.034</td>
<td>0.77nH</td>
<td>0.3pF</td>
</tr>
</tbody>
</table>

1/2 the Cpk6, 1/2 the Lpk6!
Reduction of package L:R is mostly a function of physical size. Also, elimination of the lead frame helps considerably.

QFN package connects bond pads directly to external pins

SOIC package uses leadframe to go from bond pads to external pins

Modeled 14-Pin Package-Parasitics Comparison
T-Line Neighborhood - Packaging.

A complete package model with parasitics for one driver and one receiver.