A via is a metal barrel in a PCB used to connect traces on different layers.

Vias create a parasitic capacitance to inner planes (ground or power).

The smaller the via, the less capacitance.

The current limits on via size are ≥ .008 hole while .010 is typical.

Typical via and trace:
The T-Line Neighborhood - Pcb Models

If we assume that vias have pads on inner layers also, the capacitance of a via is:

\[ C_{\text{via}} = \frac{1.41 \pi T D_{\text{pad}}}{D_{\text{clear}} - D_{\text{pad}}} \]

where

- \( D_{\text{pad}} \) = diameter of pad (in)
- \( D_{\text{clear}} \) = diameter of clearance hole (in)
- \( T \) = board thickness (in)
- \( \varepsilon_r \) = dielectric constant of board
- \( C_{\text{via}} \) = capacitance in pF

For our example (typical via):

\[ C_{\text{via}} = \frac{1.41 \pi (4.7 \times 0.062)(0.020)}{(0.024 - 0.020)} = 2 \text{pF} \quad \text{(small, 24 mil clearance hole)} \]

\[ C_{\text{via}} = \frac{1.41 \pi (4.7 \times 0.062)(0.020)}{(0.030 - 0.020)} = 0.8 \text{pF} \quad \text{(large clearance, 30 mil)} \]

Large clearances on inner layers produce a via with a smaller discontinuity

The primary effect of vias on signal traces is a slowing of the rise time due to the increased distributed capacitive loading that lowers \( Z_0 \).

For example, a string of vias occurring in a short distance could be a problem.
Vias also introduce a small inductive element that can significantly affect decoupling.

Back to the self-inductance of a wire (the via is now our wire)

\[ L = 5.08 h \left\lfloor \log \left( \frac{4h}{d} \right) \right\rfloor - 1 \]

where

- \( L \) = Inductance of via in nH
- \( h \) = Length of via (in.)
- \( d \) = Diameter of via (in.)

For a 10 mil via in .062 board:

\[ L = 5.08 (0.062) \left\lfloor \log \left( \frac{4(0.062)}{0.01} \right) \right\rfloor - 1 \]

\[ = 0.7 \text{nH} \]

Via diameter has little effect on the inductance. Via length (board thickness) makes the most difference.

Since we will often have 2 vias, one for each end of the cap, we then have:

\[ \frac{0.7 \text{nH}}{2} = 0.35 \text{nH} \]

How will this effect the performance of our decoupling capacitor?
The T-Line Neighborhood - PCB Models

Assume we have an IC operating at 3.3V, sourcing a 1ns edge into 50Ω. The voltage generated across both vias would be:

\[ V_L = L \left( \frac{di}{dt} \right) = (1.4 \times 10^{-9}) \frac{(3.3\text{ V})}{1 \times 10^{-9}} = 92\text{ mV} \]

This is fine if only output is switching. What is a switch? 92mV x 8 = 736mV not ok!

---

### State-of-the-Art Advanced BICMOS Technology (ABT) Widebus™ Design for 2.5-V and 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V \( V_{CC} \))
- Typical \( V_{OLP} \) (Output Ground Bounce) -0.8 V at \( V_{CC} = 3.3 \text{ V}, T_A = 25^\circ\text{C} \)
- High Drive
  - A Port = -12/12 mA at 3.3-V \( V_{CC} \)
  - B port = -32/64 mA at 3.3-V \( V_{CC} \)
- I/O Pin and Power-Up 3-State Support Hot Insertion
- Use Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating
- A-Port Outputs Have Equivalent 30-Ω Series Resistors, So No External Resistors Are Required
- Flow-Through Architecture Facilitates Printed Circuit Board Layout
- Distributed \( V_{CC} \) and GND Pins Minimize High-Speed Switching Noise
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

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### SN54ALVTH162245, SN74ALVTH162245
2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

### SN54ALVTH162245 ... WD PACKAGE
SN74ALVTH162245 ... DG, DGG, OR DL PACKAGE (TOP VIEW)

<table>
<thead>
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<th>3</th>
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</tr>
</tbody>
</table>

4 VSS
4 VCC
8 outputs / VCC

---

The ALVTH162245 devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for 2.5-V or 3.3-V \( V_{CC} \) operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so that the buses are effectively isolated.
Tline with one via (10mil via, .062 board, 20mil pad)

```plaintext
*input source with 5ns delay, 1ns edges, 50ns pulse width, 101ns cycle time
Vin vin 0 3.3 PULSE(0 3.3 5e-9 1n 50e-9 101e-9)
```

```plaintext
*source output impedance
rsnc vin tline_input 50
```

```plaintext
*transmission line number one, 50 ohm, 2ns electrical length
t1 tline_input 0 junction 0 z0=50 td=2ns
```

```plaintext
*transmission line number two, 50 ohm, 2ns electrical length
t2 junction 0 tline_output 0 z0=50 td=2ns
```

```plaintext
*cvia junction 0 2pF
cvia junction 0 0.8pF
```

```plaintext
.large clearance, 50 mil pad
```

```plaintext
.control
cp
tran 100ps 101ns
plot V(junction) V(tline_output) x1 5ns 20ns
```

```plaintext
set hcopydevtype=postscript
set hcopypscolor=true
set hcopydev=kec3112-clr
```

```plaintext
*color0 is background color
*color1 is the grid and text color
*colors 2-15 are for the vectors
set color0 = rgb:0/f/f
set color1 = rgb:0/0/0
set color2 = rgb:0/0/0
set color2 = rgb:f/f/f
```

```plaintext
hardcopy out.ps V(tline_input) V(tline_output) x1 0ns 20ns
.endcode
```

```
.end
```

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Friday February 2010