

Atmel Atmega128 Overview

ALU Particulars

RISC Architecture

133, Mostly single cycle instructions

2 Address instructions (opcode, Rs, Rd, offset)

32x8 Register file

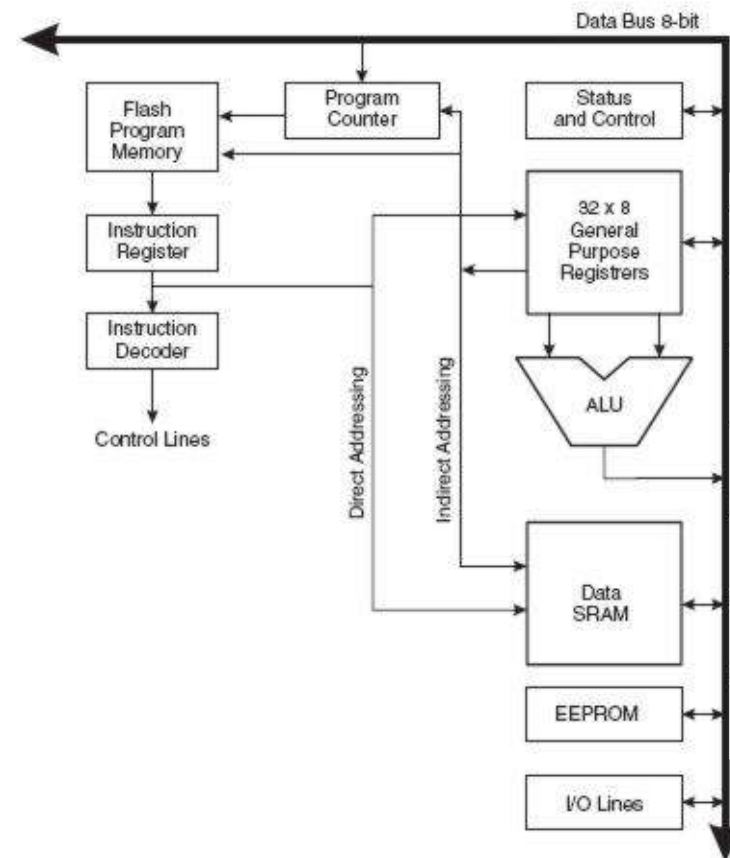
-6 can be used as 16-bit registers

Harvard architecture

Status Register

(half carry, sign, OV, Neg, Zero, Carry, GIE)

-not stored when entering ISR



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Memory System

There are four separate memory spaces on the AVR

-Program space:

- 128K byte (64Kx16) in-circuit flash programmable
- Endurance minimum of 10K cycles
- Can be accessed by program for storage of constants

-SRAM Data Memory:

- 4K bytes
- variable storage area
- i/o and peripherals are located here also

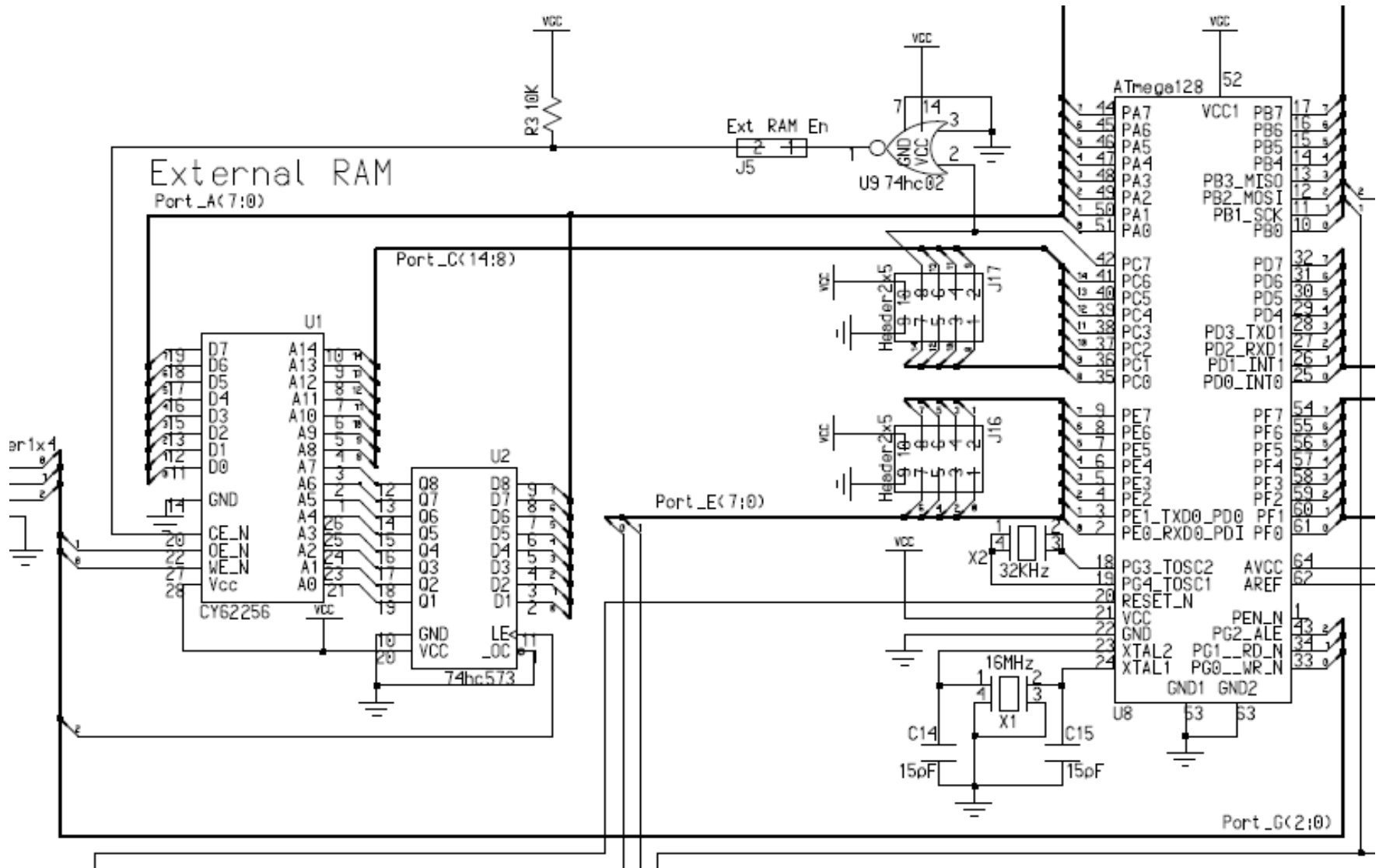
-EEPROM:

- 4K bytes
- separate data space
- single byte read/write access via EEPROM access registers
- 8.5mS to write data (slow but durable)

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Memory System

- Mega128 board has added 32K external SRAM memory
- Uses multiplexed lower address and data
- Addr bit 15 selects external memory if XMEM register is programmed



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Timers and Counters

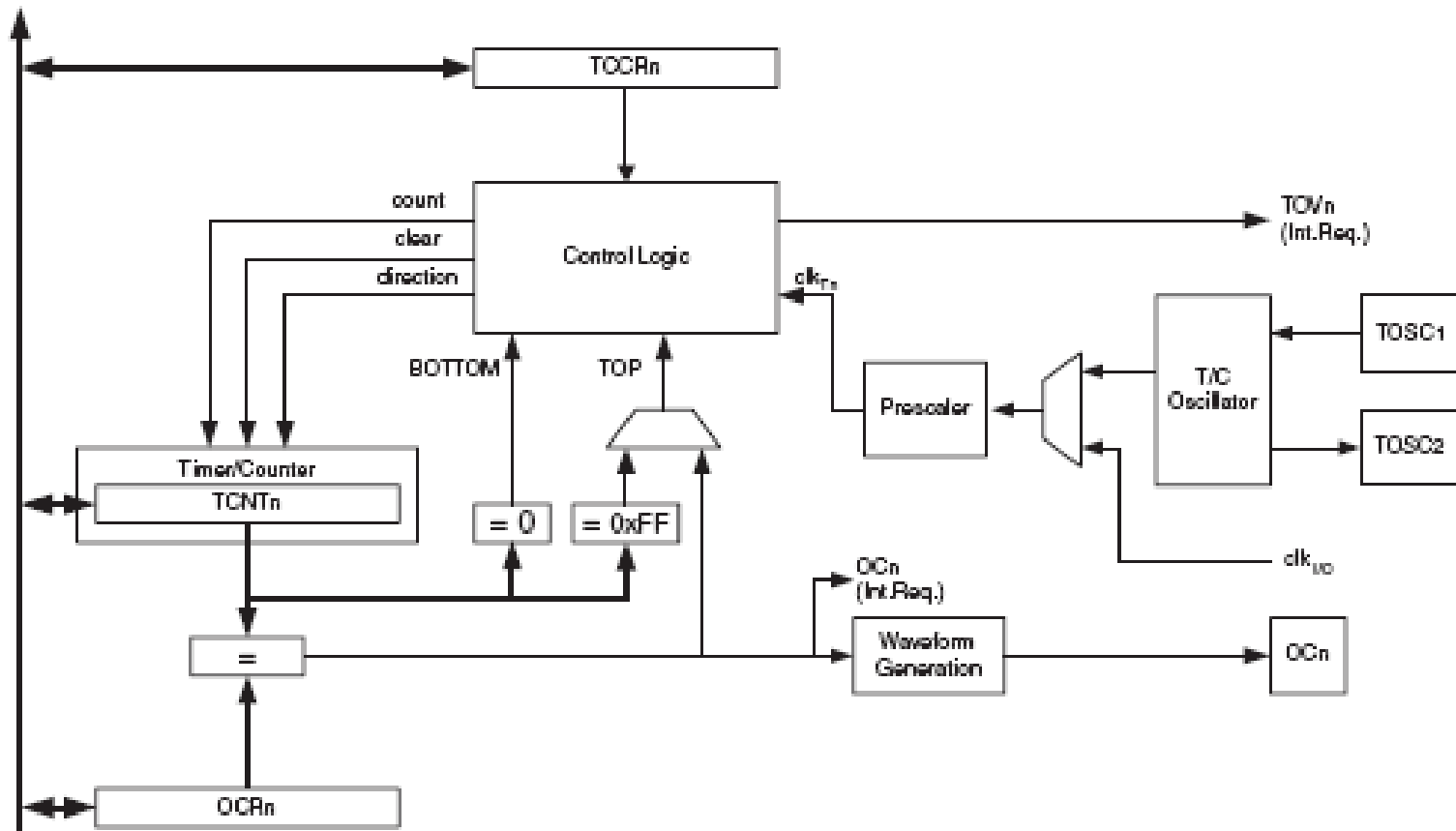
TCNT0

-8-bit

-internal synchronous clock or external asynchronous 32Khz clock

-especially used for time keeping with 32Khz clock

-has no external pin for clocking, only two crystal sources



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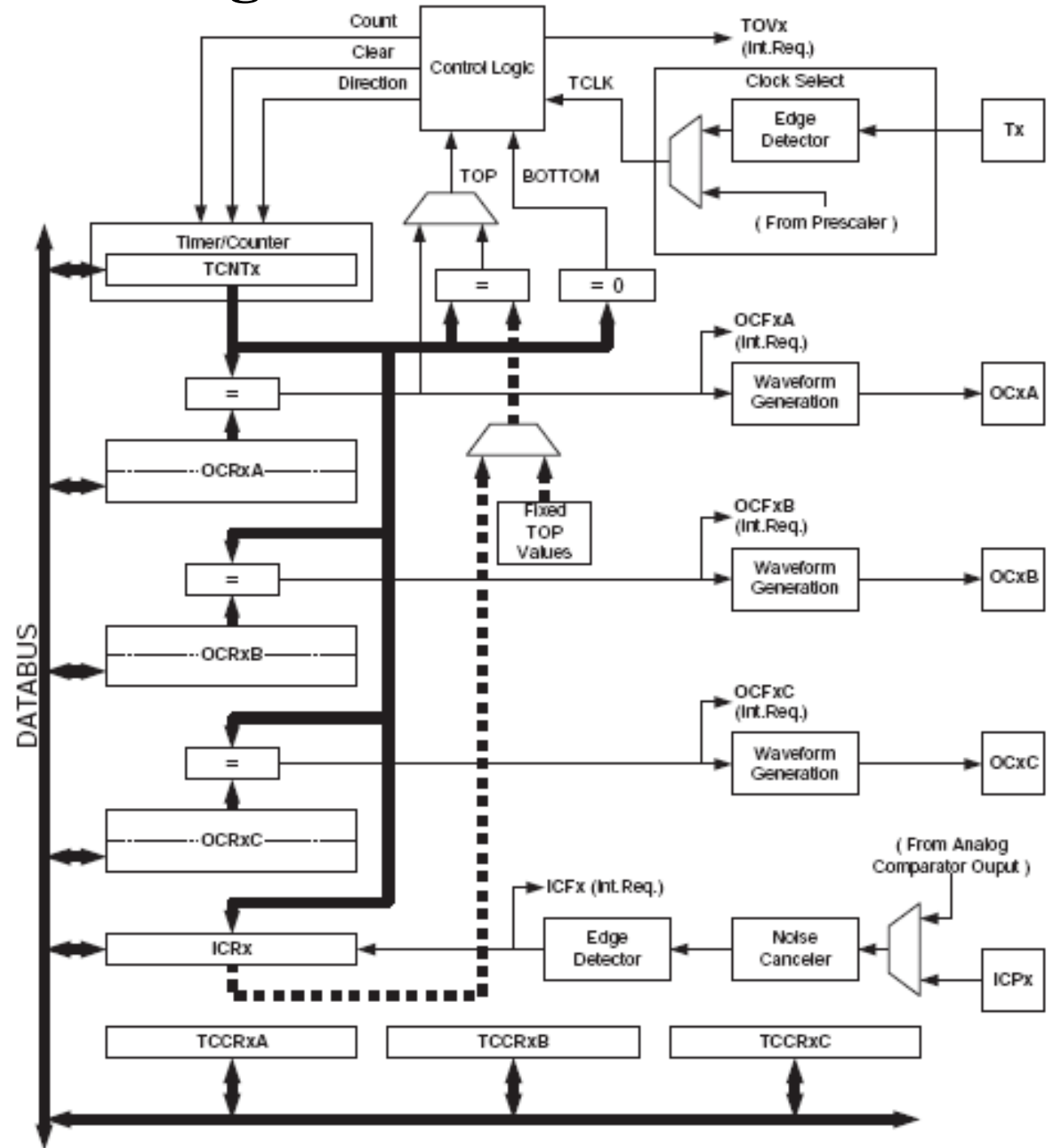
Timers and Counters

TCNT1, TCNT3

- 16 bit timer/counter, requires special access method
- clocked by internal clock or by external pin
- 3 output compare registers and output pins (set, reset, toggle)
- multiple compare registers
- input capture register captures when external event happened
- ADC interrupt input can capture time at which some voltage is detected

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Timers and Counters TCNT1, TCNT3

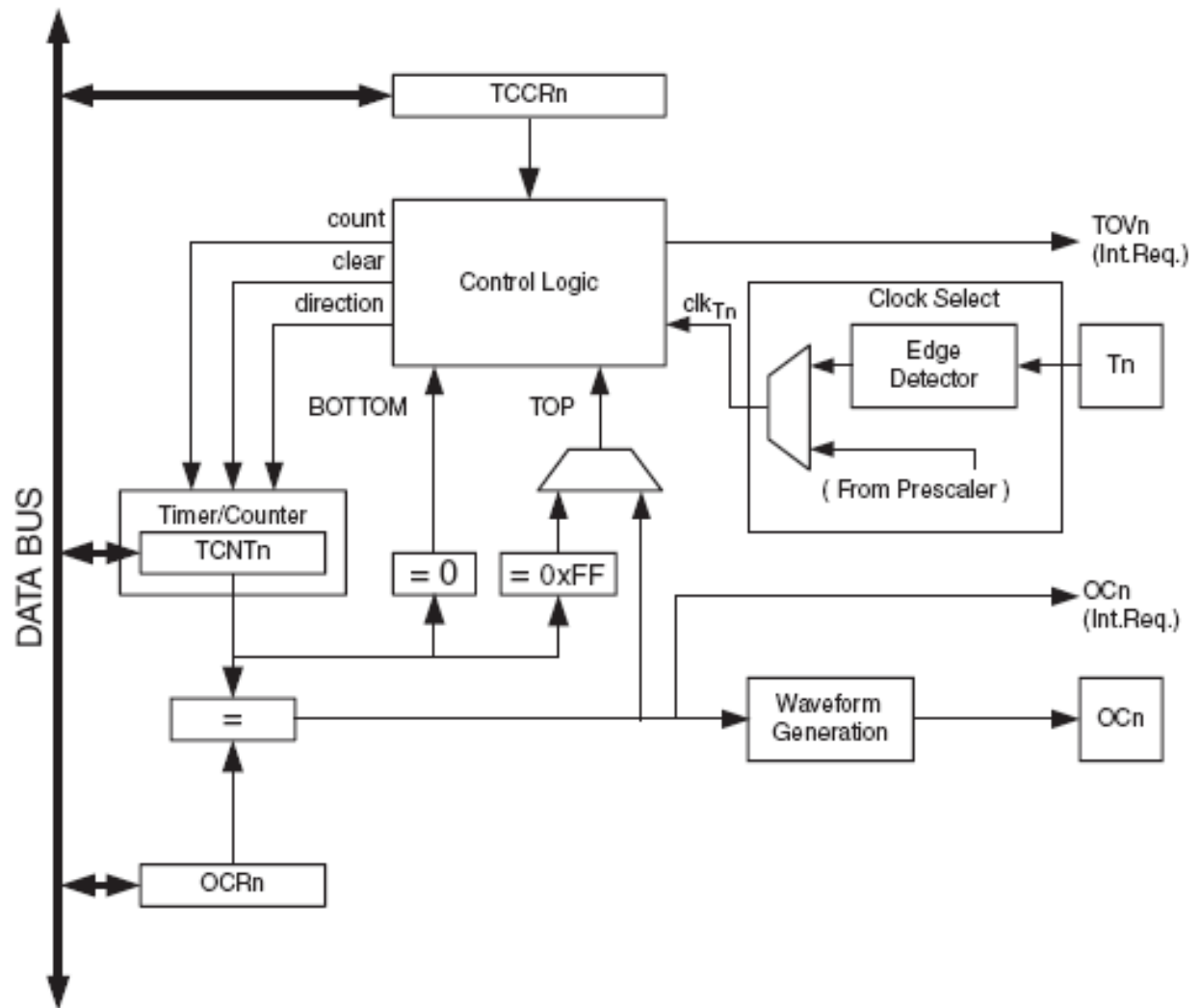


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Timers and Counters

TCNT2

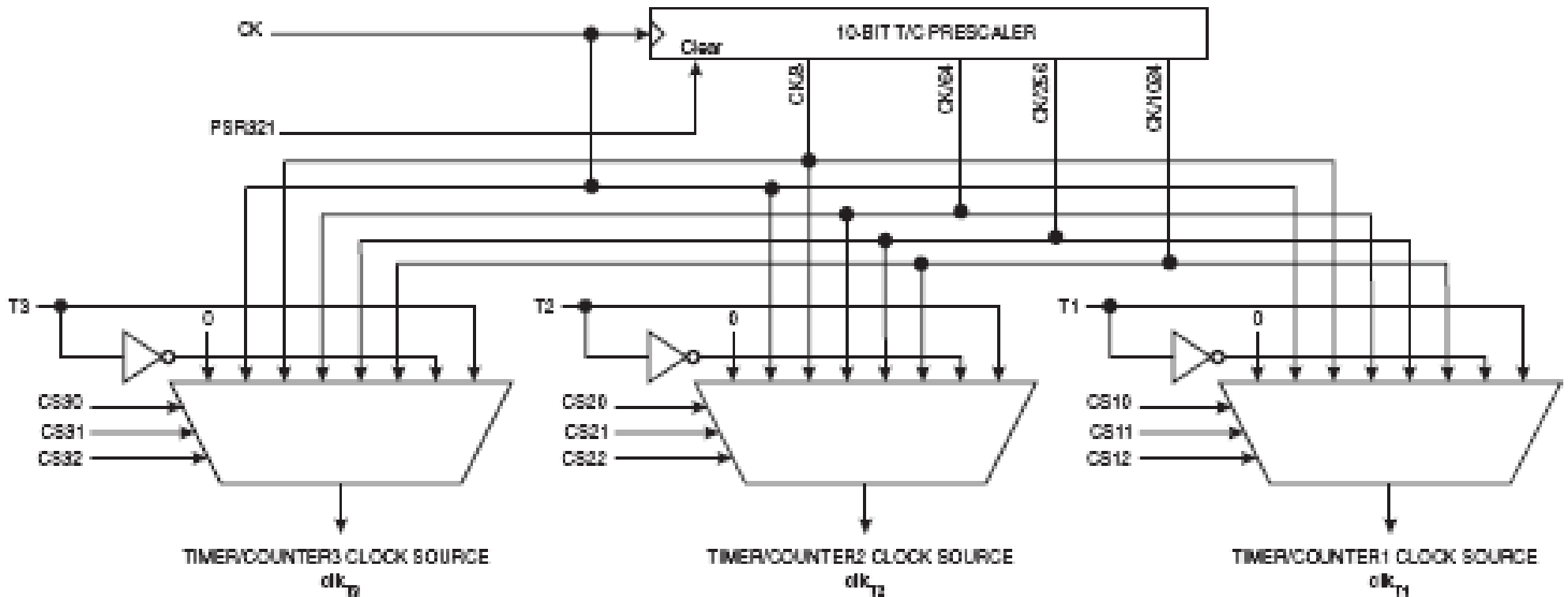
- 8-bit counter/timer
- like TCNT0 but has external clocking capability
- has PWM capability



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Timer/counter prescalers

- separate prescalers available for TCNT1,2,3 only
- used when operating from internal or external clock pin
- clock can be prescaled by 8, 64, 256 or 102



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Interrupts

30 interrupt sources

- external pin levels or edges
- timer/counters
- SPI, USART, and TWI Rx and Tx complete
- ADC conversion complete
- EEPROM ready
- input capture, external event capture, ADC interrupt

All interrupts are vectored

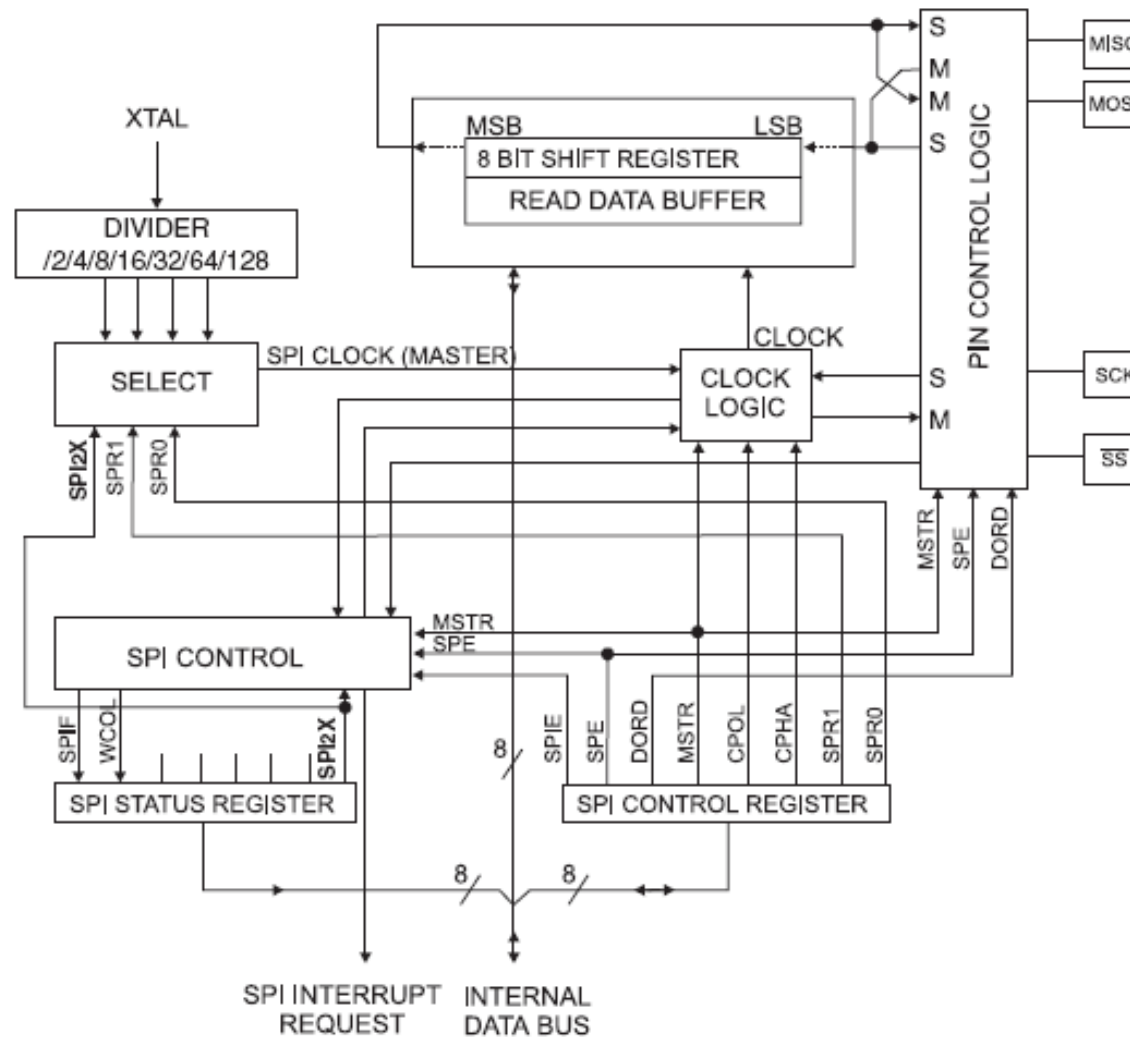
- reset is vector zero (highest priority)
- all other interrupts are prioritized in ascending order
- interrupt response time is 4 cycles
- interrupt return time is also 4 cycles

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Serial Interfaces

SPI (Serial Peripheral Interface)

- full duplex, three wire interface
- MSB first or last, programmable bit rates to $\text{clock}/2$



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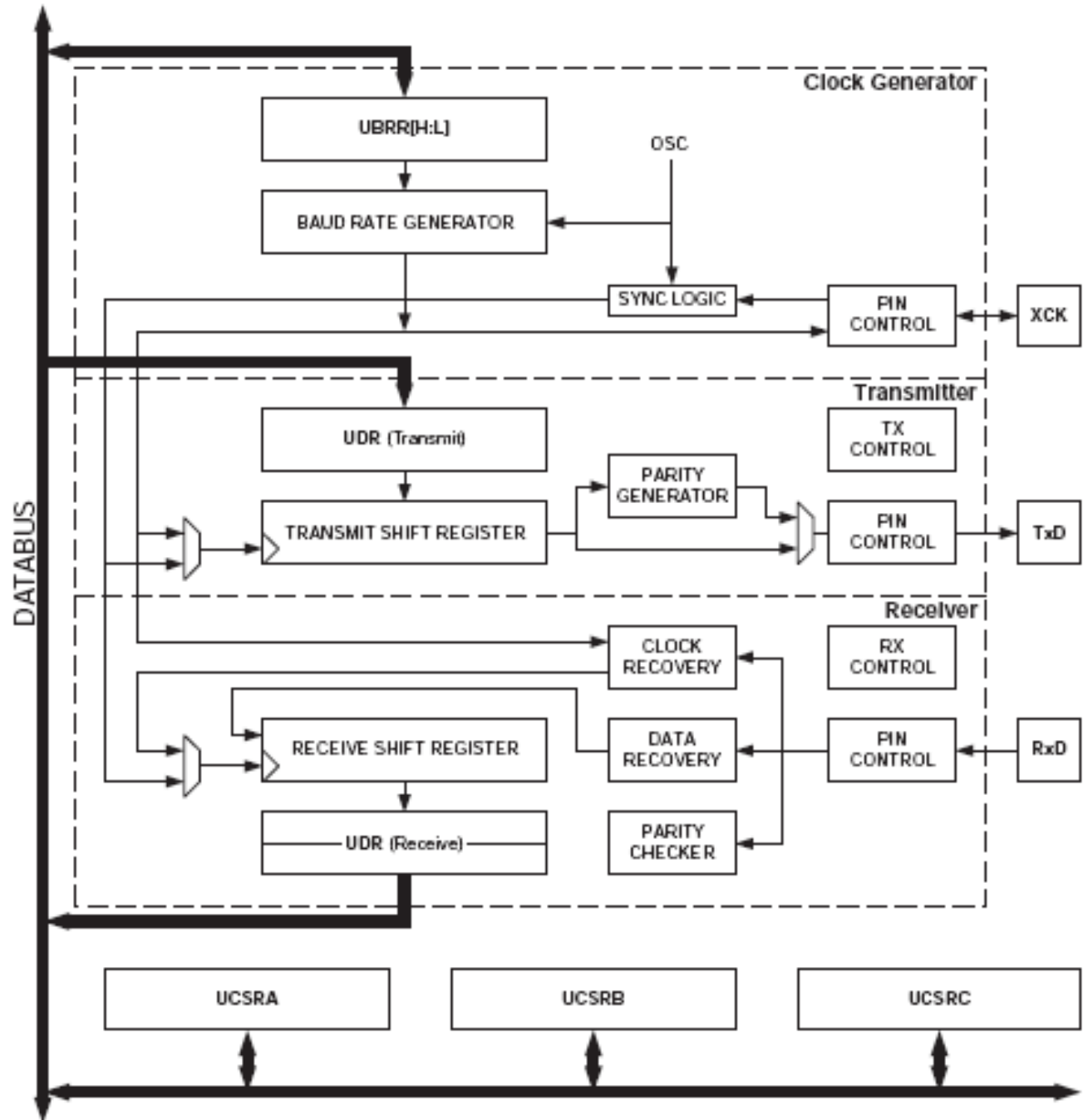
Serial Interfaces

USART(universal synchronous asynchronous receiver transmitter)

- 2 identical and separate units, USART0, USART1
- full duplex serial communications
- programmable number of bits, parity, stop bit, error detection
- interrupt on tx done, rx ready, or tx register empty

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Serial Interfaces USART0,1



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Serial Interfaces

TWI (two wire interface)

- half duplex serial communications
- 7 bit device addressing
- multi-master operation
- 400khz data rate
- I²C compatible

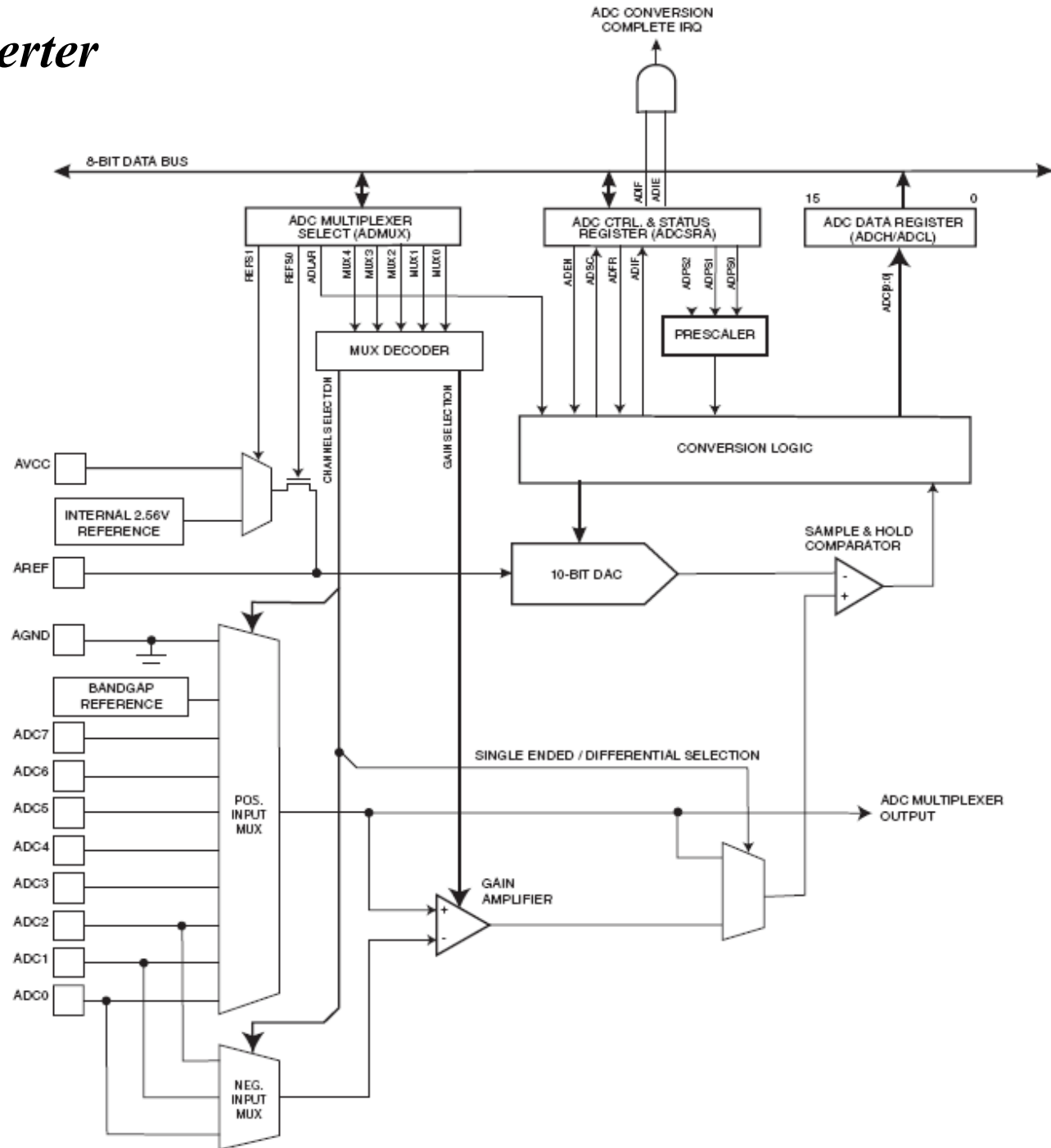
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Analog to Digital Converter

- 10-bit resolution
- 13-260uS conversion time
- 8 multiplexed single input channels
- 7 differential input channels
- selectable internal reference (2.56V)
- input range 0-V_{cc}
- interrupt on completion

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Analog to Digital Converter



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