The JTAG (Joint Test Action Group) development started about 1985 as a method to test populated circuit boards after manufacture.

The majority of manufacturing and field faults in circuit boards were due to bad solder joints.

JTAG was meant to provide a “pins-out” view from one IC pad to another so all these faults could be discovered.

Became an IEEE standard in 1990 (IEEE Std. 1149.1-1990)

Now adopted by electronics companies all over the world.

*Boundary-scan* is mostly synonymous with JTAG.

In many ICs, internal registers are on a *scan chain*. This allows functionality to be tested completely even while an IC is in the circuit card and possibly while in a functioning system.
In the most basic implementation, the boundary that is scanned is the i/o shell at the periphery of a chip.

The interfaces to the JTAG logic are very similar to what we have seen for SPI.....

tck  equiv to  sck
tdi  equiv to  mosi
tdo  equiv to  miso
tms  no match

The JTAG scan chain forms a long shift register.
AVR JTAG Interface

Boundary scan principle of operation - chip level

Each boundary-scan cell can:
- **Capture** data on its parallel input PI
- **Update** data onto its parallel output PO
- **Serially scan** data from SO to its neighbour’s SI
- Behave **transparently**: PI passes to PO
- Note: all digital logic is contained inside the boundary-scan register
AVR JTAG Interface

Boundary scan principle of operation  - board level
AVR JTAG Interface

JTAG is now primarily used as
- a method to access sub-blocks of integrated circuits
- programming non-volatile memories (EEPROM, Flash)
- a mechanism for debugging embedded systems
- a mechanism for checking for manufacturing defects

As a debugging tool, an *in-circuit emulator* enables a programmer to access an on-chip debug module integrated into the CPU.

The debug module enables the programmer to debug the software of an embedded system by setting breakpoints, view CPU registers and other internal registers.

The JTAG scan chain generally does not help diagnose or test for timing, temperature or other dynamic errors.
AVR JTAG Interface

JTAG on the AVR allows access to:
- all internal peripheral units
- internal and external RAM
- internal register file
- program counter
- EEPROM and Flash memory

With the AVR Studio, on chip debug is supported for:
- AVR “BREAK” instruction
- break on change of program memory flow
- single step break
- memory breakpoints

On-chip debug is via private JTAG instructions (Atmel proprietary)
AVR JTAG Interface

ICE with AVR

AVR JTAGICE mkII

Description:
The AVR® JTAGICE mkII from Atmel® is a powerful development tool for On-chip Debugging of all AVR 8-bit RISC microcontrollers with IEEE 1149.1 compliant JTAG interface or debugWIRE Interface. debugWIRE enables on-chip debug of AVR microcontrollers in small pin count packages, using only a single wire for the debug interface.

The AVR Studio online-help contains the most current information and a complete list of supported devices.

Ordering Code: ATJTAGICE2

Documents:
AVR JTAG Interface

JTAG on the AVR: