AVR Reset Sources

When a reset event occurs....
   -I/O registers set to initial values immediately
    -internal delay stretched to allow power to stabilize
    -PC loaded with reset vector (containing jmp to reset handling routine)

There are 5 sources of reset:
    -Power-on Reset: Vcc is below Vpot
    -External Reset: Low level assertion on reset_n pin for 1.5uS
    -Watchdog Reset: Watchdog timer expires
    -Brown-out Reset: Vcc briefly drops below Vbot
    -JTAG AVR Reset: Reset command is scanned into JTAG

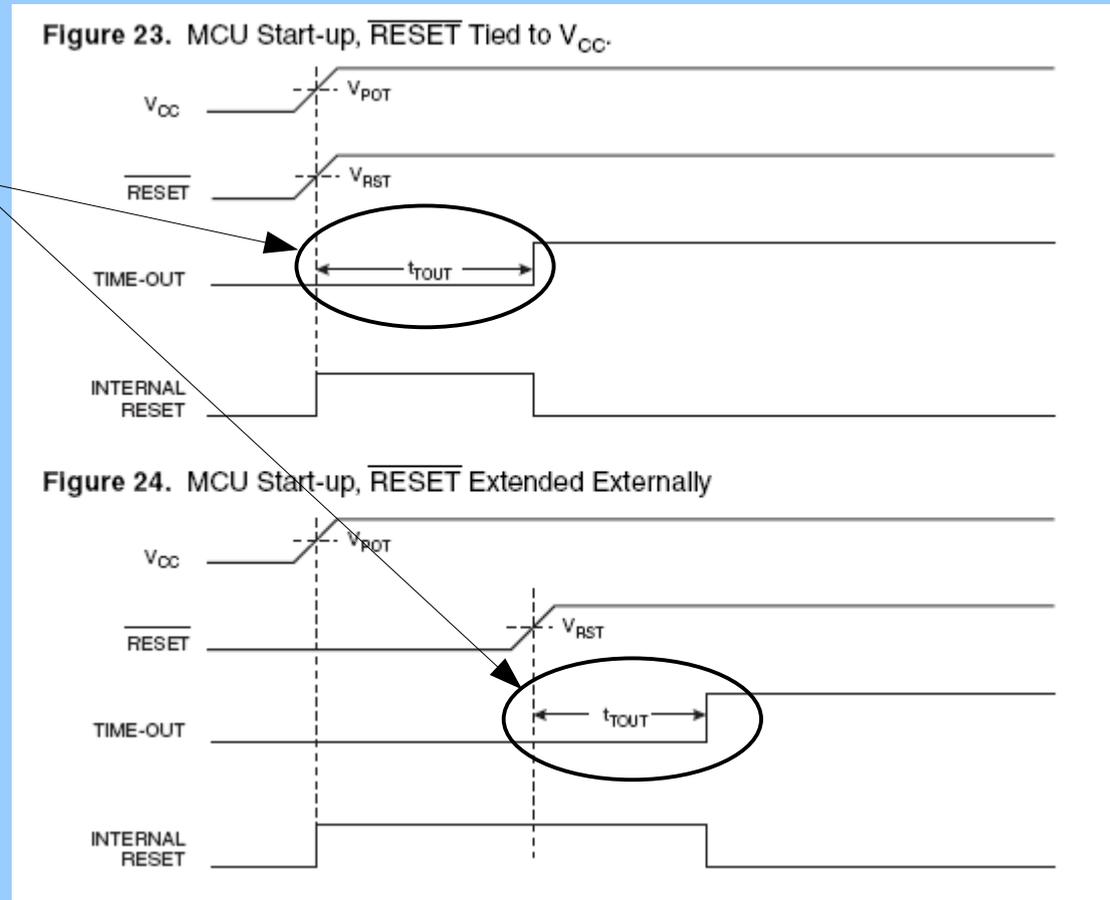# AVR Reset Sources
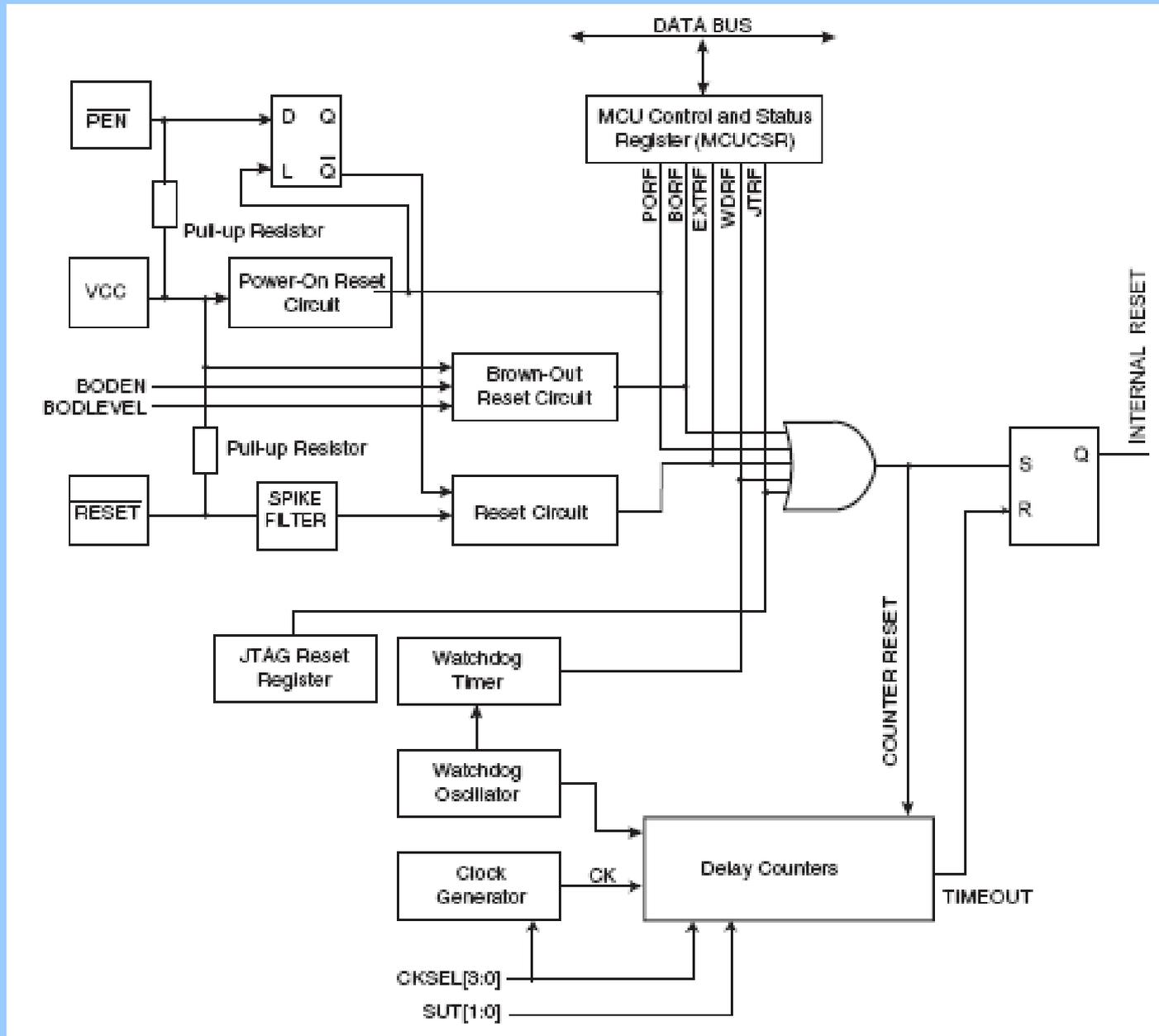
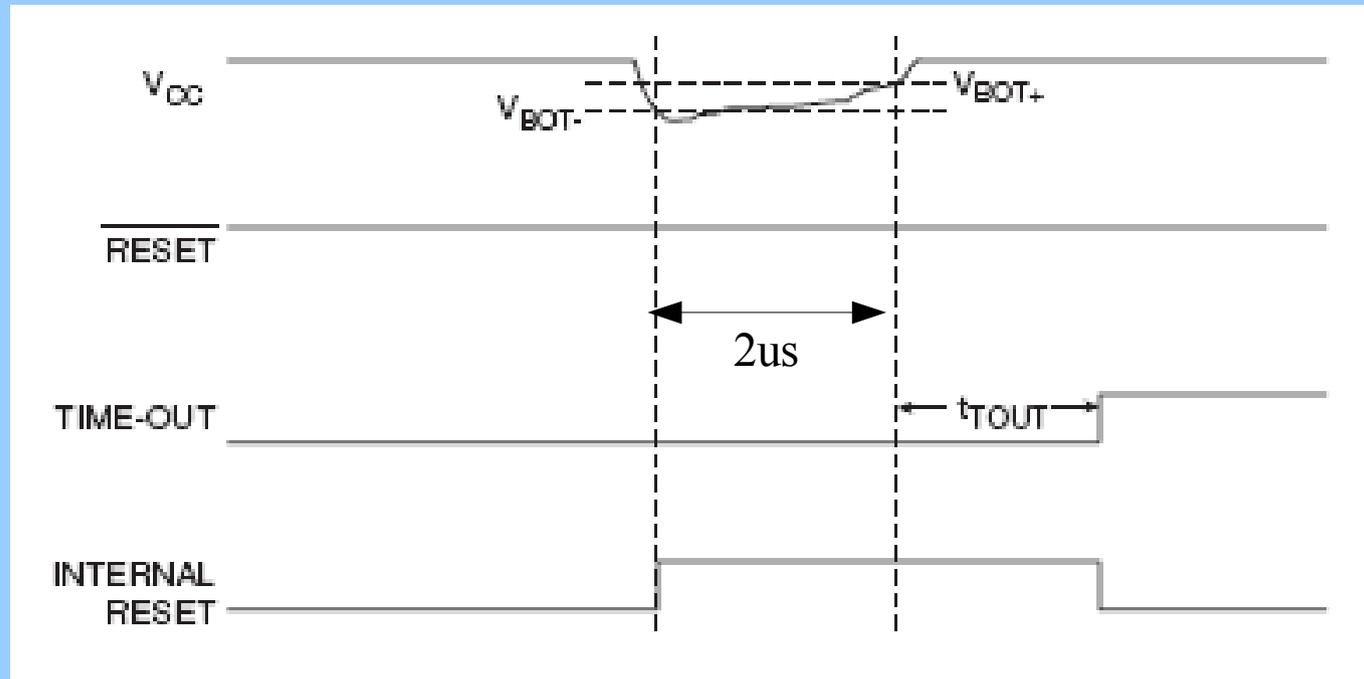## AVR Reset Logic

AVR Reset Sources

AVR Reset Logic Operation

Watchdog timer used to determine how much delay to add after reset_n deasserts.

This is set by the AVR fuses to be either 4.1ms or 65ms.

Figure 23. MCU Start-up, $\overline{RESET}$ Tied to V_{CC}.

Figure 24. MCU Start-up, $\overline{RESET}$ Extended Externally

AVR Reset Sources

AVR Brownout Operation

Brown out detection (BOD) level can be set to 2.7V or 4.0V.

Vcc must droop below the Vbod- level for more than 2uS.

BOD circuit has 100mV hysteresis to prevent reset due to glitches

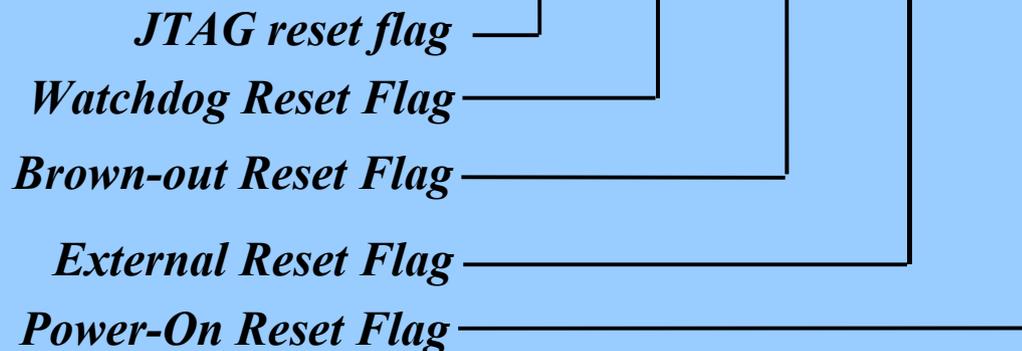BOD must be enabled by programming the BOD fuse.

AVR Reset Sources

Who cut out the lights?

Determining what the source of the reset was can be useful to self diagnostic software.

The MCU Control and Status Register MCUCSR provides information as to the source of the reset that most recently occurred.

Bit	7	6	5	4	3	2	1	0	
	JTD	–	–	JTRF	WDRF	BORF	EXTRF	PORF	MCUCSR
Read/Write	R/W	R	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0		See Bit Description				

JTAG reset flag

Watchdog Reset Flag

Brown-out Reset Flag

External Reset Flag

Power-On Reset Flag

AVR Reset Sources

Watchdog timer

A watchdog timer is a hardware resource that can help an errant program get back on track.

The program must periodically reset the watchdog timer before it goes off.

If the timer goes off, the uC and hopefully all peripherals are reset.

The timer should be difficult to reset except by a well behaving software.

AVR Reset Sources

Watchdog timer

The AVR watchdog timer is clocked by a separate on-chip 1Mhz oscillator.

Eight separate clock cycle times can be chosen.

The watchdog timer is reset by the *Watchdog Reset* instruction *WDR*.

If the timer times out, the uC is reset just as if power had been removed and reapplied.

There are three safety levels you can set the watchdog timer to.

The safety levels are programmed by fuse bits. These cannot be changed unless the part is reprogrammed.

AVR Reset Sources

Watchdog Timer Control Register (WDTCR)

Bit	7	6	5	4	3	2	1	0	
	–	–	–	WDCE	WDE	WDP2	WDP1	WDP0	WDTCR
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

watchdog change enable:
Must be set when WDE is set to zero. If written to
one, HW will clear within 4 clock cycles

watchdog enable: When logic one, watchdog is
enabled, when zero disabled. Can only be cleared
when WDCE bit is also set.

To disable a watchdog timer: (impossible in safety level 2)
1. Simultaneously write logic one to WDCE and WDE
2. Within 4 cycles write WDE logic 0
   (this is called a "timed sequence)

watchdog timer prescaler: determines prescaling
for watchdog timer

AVR Reset Sources

Watchdog timer safety levels

Safety level 0:
    WDT initially disabled
    Can be enabled by writing WDE bit to 1 without any restriction
    Timeout period can be changed at any time
    To disable:
        -Simultaneously, write a logic 1 to WDCE and WDE
        -Within 4 clock cycles, write WDE to logic 0

Safety level 1:
    WDT Initially disabled
    Can be enabled by writing WDE bit to 1 without any restriction
    Timeout or disable requires timed sequence
    To disable or change timeout:
        -Simultaneously, write a logic 1 to WDCE and WDE
        -Within 4 clock cycles, write WDE and WDP bits as desired
          but with WDCE bit cleared

AVR Reset Sources

Watchdog timer safety levels

Safety level 2:
    WDT initially enabled, WDE bit always reads logic one
    WDT cannot be disabled
    Timeout can be changed, but requires timed sequence
    To disable or change timeout:
        -Simultaneously, write a logic 1 to WDCE and WDE
        -Within 4 clock cycles, write WDP bits as desired with
          WDCE bit cleared. WDE bit value is irrelevant.