Capacitance Meter Using ATmega128 ECE 473, Fall 2014

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Motivation

Capacitor tolerances are commonly $\pm 20\%...$ does this matter?

- Digital applications
 - Usually just a decoupling cap, precise value doesn't matter
- Analog applications X
 - Used in filters, for which cutoff frequency is important
 - ▶ Matching requirements in data converters often < 0.1%
 - Exacerbated in high-frequency PLLs and RF transceivers

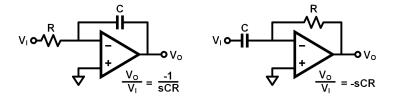


Figure 1: Examples of capacitors used in integrator (left) and differentiator (right)

I-V Characteristics of Capacitor

Integral form of capacitor voltage:

$$V(t) = rac{1}{C} \int_{t_0}^t I(au) d au + V(t_0)$$
 $C = rac{1}{V(t) - V(t_0)} \int_{t_0}^t I(au) d au$

Two assumptions to greatly simplify this: constant current $I(\tau) = I_O$, and initial condition $V(t_0) = 0$. Then:

$$C = rac{1}{V(t)} \cdot I_O \cdot (t - t_0)$$
 $C = rac{I_O \cdot \Delta t}{V(t)}$

I-V Characteristics of Capacitor

$$C = \frac{I_O \cdot \Delta t}{V(t)}$$

Two options to measure unknown C:

- 1) Measure V(t) after fixed Δt
 - Some fixed delay using timer
 - Use analog-to-digital (ADC) to read V(t)
 - $ightharpoonup C \propto rac{1}{V(t)} X$

- 2) Count Δt to reach fixed V(t)
 - Fixed threshold voltage with analog comparator
 - ightharpoonup Count Δt with timer
 - $ightharpoonup C \propto \Delta t \checkmark$

Analog Comparator within ATmega128

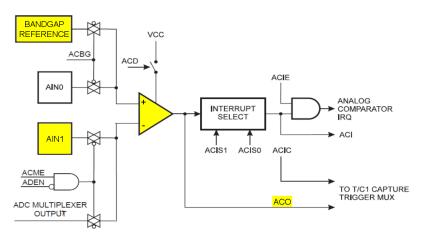


Figure 2: Analog Comparator block diagram¹

Q: What is so great about having a bandgap reference?

¹ATmega128 Datasheet (2011), p. 227

Comparator Output Waveform

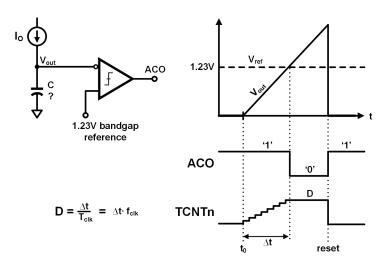


Figure 3: Using analog comparator to track charging progress

Implementing DC Current Source

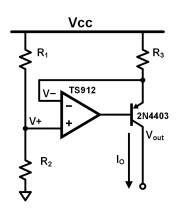


Figure 4: Providing constant current with opamp

Main points:

- 1. Feedback path forces $V_+ = V_-$
- 2. Voltage drop over *R*₃ determines output current
- BJT acts as unity-gain current buffer
- 4. Works well for $V_{out} < V_{-} V_{ECsat}$
 - $R_2 = 10 \cdot R_1$ gives large headroom

$$I_O = \frac{V_{cc} - V_{-}}{R_3} = \frac{V_{cc} - V_{+}}{R_3}$$
$$= \frac{V_{cc} - (\frac{10}{11})V_{cc}}{R_2} = \frac{V_{cc}}{11 \cdot R_2}$$

Determining D→C Transfer Function

From before:

$$C = \frac{I_O \cdot \Delta t}{V(t)}$$

where

$$\Delta t = \frac{D}{f_{clk}} \qquad I_O = \frac{V_{cc}}{11 \cdot R_3}$$

Then transfer function is given by:

$$C = \frac{V_{cc} \cdot D}{11 \cdot R_3 \cdot V_{ref} \cdot f_{clk}}$$

Determining D→C Transfer Function

Assuming $V_{cc} = 5V$ and with $R_3 = 1k$:

$$C = \frac{5 \cdot D}{11 \cdot 1k \cdot 1.23 \cdot 16M} = (2.30968 \cdot 10^{-11})D \quad [F]$$
$$= 0.0230968 \cdot D \quad [nF]$$
$$10 \cdot C = 0.230968 \cdot D \quad [nF]$$

- ▶ For digital arithmetic, calculating 10 C makes result "look like" floating point number
 - Just insert decimal point before writing to LCD
- ▶ D comes from 16-bit TCNTn, so range is 23pF to 1.5μ F

Q: What are two ways to change this range?

Final Hardware Design

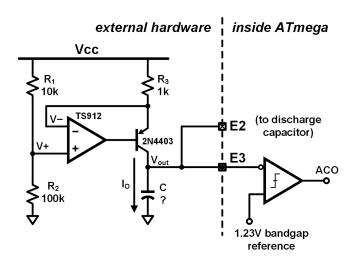


Figure 5: Schematic of capacitance meter with ATmega128

Sources of Error

- Offset errors
 - Capacitor doesn't fully discharge
 - Counter starts before capacitor starts charging
 - Equivalent series resistance (ESR)
 - ▶ I/O pin contributes some fixed capacitance
- Gain errors
 - Supply voltage variations
 - Component tolerances
- Nonlinearity
 - Current source nonlinearity
 - Capacitance may change with voltage

Sources of Error

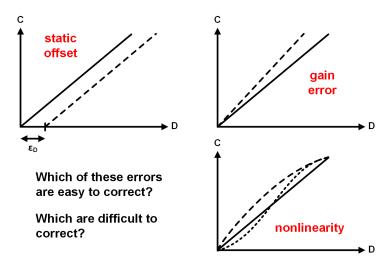


Figure 6: Illustration of $D\rightarrow C$ errors

Calibrating Errors

$$C = m \cdot (D - \epsilon_D)$$

- ▶ Static offset: ϵ_D is count when C=0
- Gain error: nominally 0.230968, but can be determined experimentally using well-known capacitor values
- ▶ Nonlinearity: sometimes implemented as piece-wise gain error, or as a look-up table
 - Generally a more complicated beast, outside the scope of this discussion

Relevance to ADC Design

Alternatively, suppose that C is known and reference voltage is unknown V_{IN} :

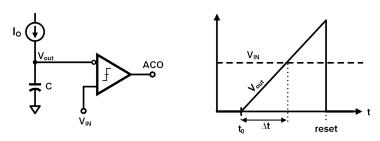


Figure 7: Capacitance meter reconfigured as ADC

ADC transfer function looks like:

$$V_{IN} = \frac{I_O \cdot D}{C \cdot f_{cIk}}$$

Relevance to ADC Design

Integrating quantizer is one of many ADC architectures. Others include:

- Flash
- Pipeline
- Successive Approximation
- Incremental
- \triangleright $\Delta\Sigma$ modulator

ADCs are *inherently* mixed-signal design... requires background in both analog (ECE 422/423/520) and digital (ECE 46x/471/474) circuits, as well as scripting (MATLAB, Bash, HSpice).