AVR Freaks

DESIGN NOTE #045

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KEYWORDS: SHIFT REGISTERS, PORT EXPANTION, SPI

Using Shift Registers to Increase the Number of Input/Output Pins

Introduction

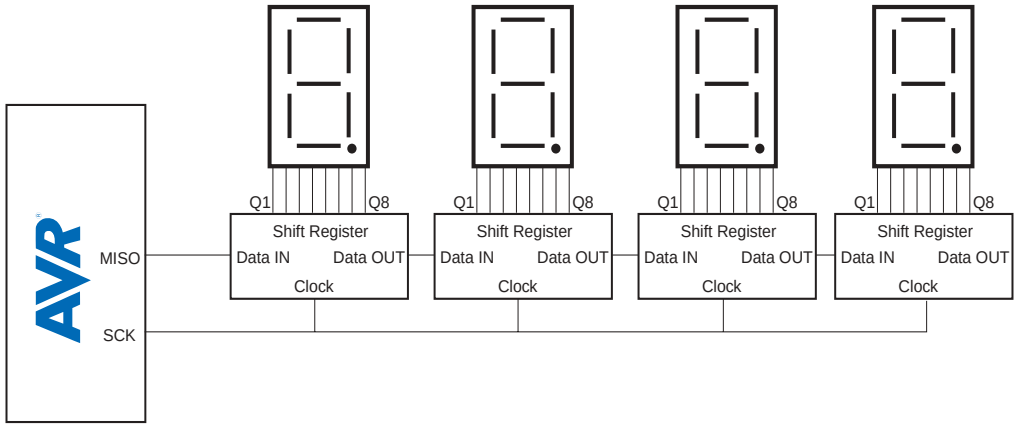
Inevitably during the design of a microprocessor based device a larger than desired microprocessor is chosen because of the high number of I/O lines required. In this design note we shall look at Shift Registers as a mean of increasing the number of I/O lines.

Overview

The SPI port on most AVR micros is ideal for controlling Shift Registers. Even if you don't have an SPI port you can still bit-bang the data out using normal I/O pins.

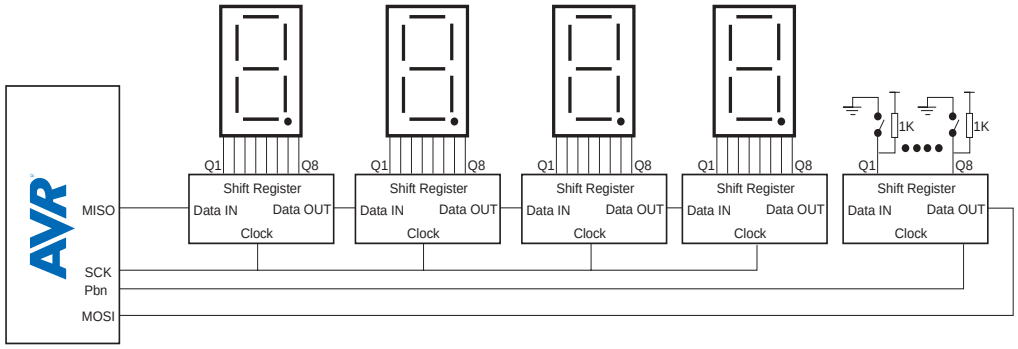
Below are some examples of the use of Shift Registers.

Figure 1. Example One of Shift Resgister Use



In the Figure 1 example each of the digits required are simply loaded in turn into the SPI Data Register and shifted out in turn. Because the SPI data rate is so high the update will not be seen by the human eye and the processor is not burdened by the multiplexing task, not to mention that only two pins were used.

Figure 2. Example Two of Shift Resgister Use



In Figure 2 a Shift Register with a PL (Parallel Load) pin is used to serve as a keyboard input stage.

The data can be shifted into the seven segment displays while at the same time reading the switches.

Here is a sequence to achieve this task:

1. Toggle PBn to latch the switch settings into the Shift Register on the far right.
2. Place the least significant digit into the SPI TX Register and shift the byte out.
3. Read the received byte in the SPI RX Register which is the switch settings.
4. Place the next three digits into the SPI TX Register in turn and shift them out.

This Shift Register technique can also be used to set up addresses to large amounts of Static RAM.

32K and 64K Static RAM chips are relatively cheap these days and unlike DRAM can easily be memory backed up.

The important thing to realise though is that only devices which are synchronous can be controlled this way.

For example if the 32 Static RAM chip were to be left enabled and in Write mode while the address was being clocked in you would corrupt 16 other locations on your way to setting up the right address.

It is also important to realise that even though some devices may not seem suitable to be controlled in this manner sometimes they can. For example lets take a garden watering system with relays used to activate the water valves. Normally you would not want them to turn on and off as the new watering combination is clocked into the Shift Register, however relay dynamics prevent them from responding to any glitches over 1 kHz and thus will not be affected by the >100 kHz SPI clock rate.