ECE473 Quiz 6 11/10/2008

Name: KEY

1. [40] A project needs the use of a voltage comparator. It must signal logic true if an input voltage is greater than 2.5 volts and output the digital decision to an electrical pin. Speed and absolute accuracy is not an issue. Unfortunately, there is no room on the PCB to add a comparator. However, a ATmega128 is on the board and has port E, bit 3 as well as port B, bit 0 available. The AIN0 pin is not available to the comparator.

Implement a system using interrupts to provide this function. Show the schematic diagram, including the input, output and any external circuitry. Label all port pins and resistor values. Code the interrupt service routine. The output is to be initialized to zero. Registers that do not need to be changed can be marked "no change".

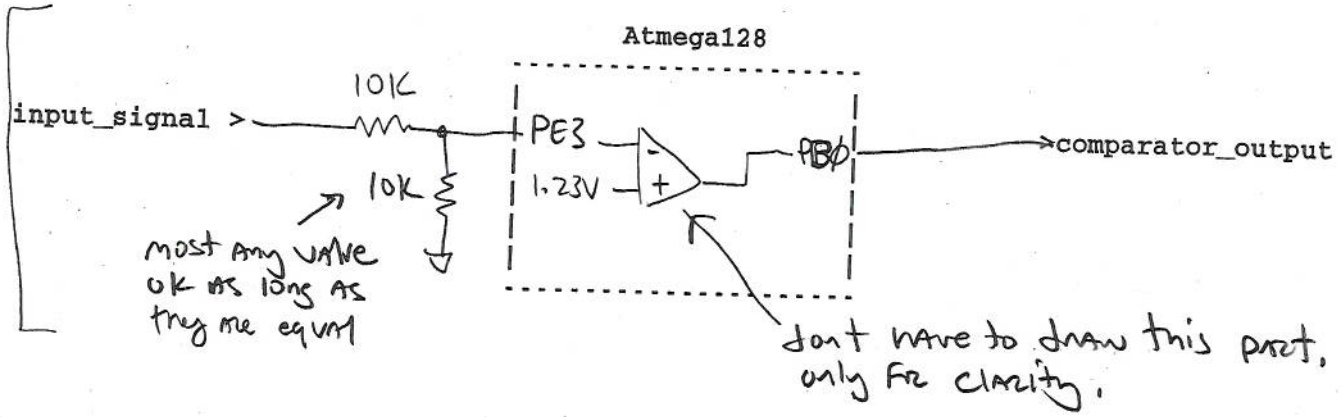
[6]
```
ISR(ANALOG_COMP_vect ){
```

[12]
```
//ISR code goes here
IF( bit_is_set(ACSR,ACO)){PORTB &= ~(0x01);}
else {PORTB |= (0x01);}

}//end ISR
```

[4]
```
main(){
DDRE &= ~(1<<PE3);
PORTE &= ~(1<<PE3);
DDRB |= (1<<PB0);
PORTB &= ~(1<<PB0);
```

[8]
```
//comparator setup
SFIOR No change
ACSR |= (1<<ACBG) | (1<<ACIE);
sei();

while(1){ }
}//end main()
```

[10]



(in single-shot mode)

2.[20] The ATmega128 ADC is being used to measure an signal that varies from 0 to 2.50V. Show the setup that will allow for the greatest resolution and the fastest conversion time while running the ADC at less than 200khz. The only external voltage available to the chip is 5 volts. Measurement is to be taken single ended at ADC7. No external circuitry is allowed. No interrupts are needed. The system clock is 4Mhz.

```
ADMUX  |= (1<<REFS1) | (1<<REFS0) | (1<<MUX2) | (1<<MUX1) (1<<MUX0
ADCSRA |= (1<<ADEN) | (1<<ADPS2) | (1<<ADPS0)
```

3.[10] A USART is sending data to another USART. The following data bytes are received at the receiver. Place an arrow adjacent to the two bytes that are in error. The channel is setup as: 8 data bits, one parity bit, and one stop bit.

start								stop		
0	1	0	1	1	0	1	1	1	0	E
0	0	0	1	0	0	1	0	1	0	O ← ERROR [5]
0	1	1	0	1	1	0	1	1	0	E
0	0	1	1	0	0	1	0	1	0	E
0	0	1	0	1	1	0	1	0	0	E
0	1	0	0	0	1	0	1	0	1	E
0	0	1	1	1	0	1	1	1	1	O ← ERROR [5]
0	0	0	0	1	1	0	0	0	0	E
0	1	0	0	1	1	0	1	1	1	E

MUST BE USING EVEN PARITY.