29. DAC – Digital to Analog Converter

29.1 Features

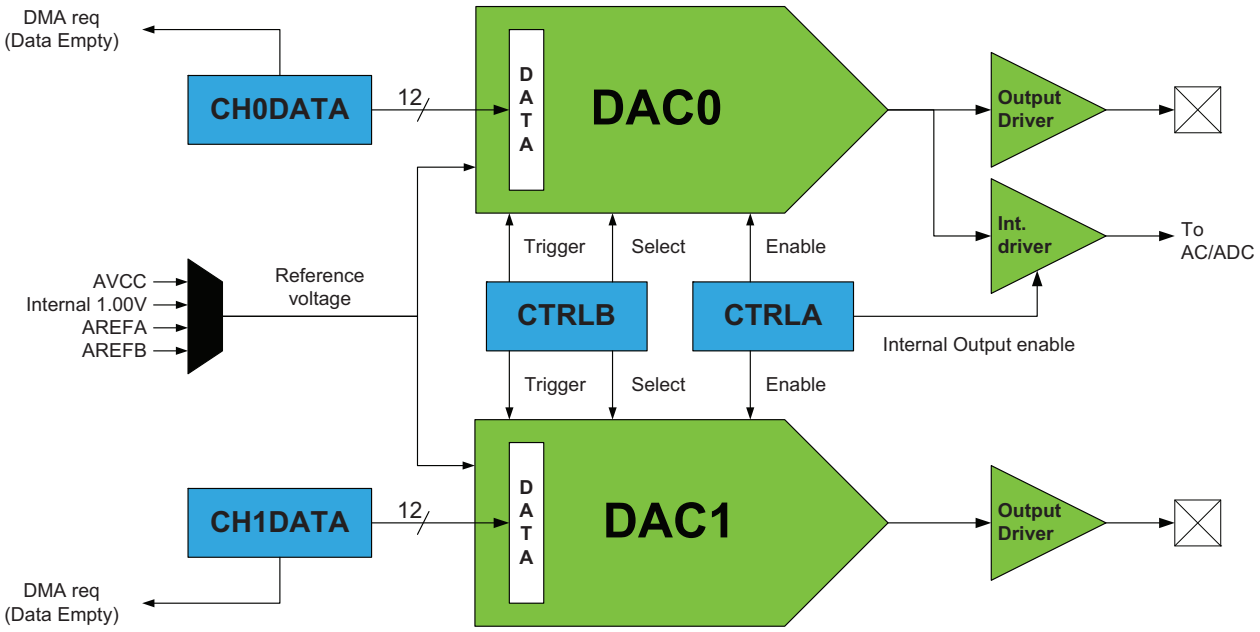
- 12-bit resolution
- Two independent, continuous-drive output channels
- Up to one million samples per second conversion rate per DAC channel
- Built-in calibration that removes:
  - Offset error
  - Gain error
- Multiple conversion trigger sources
  - On new available data
  - Events from the event system
- High drive capabilities and support for
  - Resistive loads
  - Capacitive loads
  - Combined resistive and capacitive loads
- Internal and external reference options
- DAC output available as input to analog comparator and ADC
- Low-power mode, with reduced drive strength
- Optional DMA transfer of data

29.2 Overview

The digital-to-analog converter (DAC) converts digital values to voltages. The DAC has two channels, each with12-bit resolution, and is capable of converting up to one million samples per second (MSPS) on each channel. The built-in calibration system can remove offset and gain error when loaded with calibration values from software.

Figure 29-1 illustrates the basic functionality of the DAC. Not all functions are shown.

Figure 29-1. DAC overview.



A DAC conversion is automatically started when new data to be converted are available. Events from the event system can also be used to trigger a conversion, and this enables synchronized and timed conversions between the DAC and other peripherals, such as a timer/counter. The DMA controller can be used to transfer data to the DAC.

The DAC has high drive strength, and is capable of driving both resistive and capacitive loads, as well as loads which combine both. A low-power mode is available, which will reduce the drive strength of the output.

Internal and external voltage references can be used. The DAC output is also internally available for use as input to the analog comparator or ADC.

29.3 Voltage reference selection

The following can be used as the reference voltage (VREF) for the DAC”

- AV_{CC} voltage
- Accurate internal 1.00V voltage
- External voltage applied to AREF pin on PORTA
- External voltage applied to AREF pin on PORTB

29.4 Starting a Conversion

By default, conversions are started automatically when new data are written to the channel data register. It is also possible to enable events from the event system to trigger conversion starts. When enabled, a new conversion is started when the DAC channel receives an event and the channel data register has been updated. This enables conversion starts to be synchronized with external events and/or timed to ensure regular and fixed conversion intervals.

29.5 Output and output channels

The two DAC channels have fully independent outputs and individual data and conversion control registers. This enables the DAC to create two different analog signals. The channel 0 output can also be made internally available as input for the Analog Comparator and the ADC.

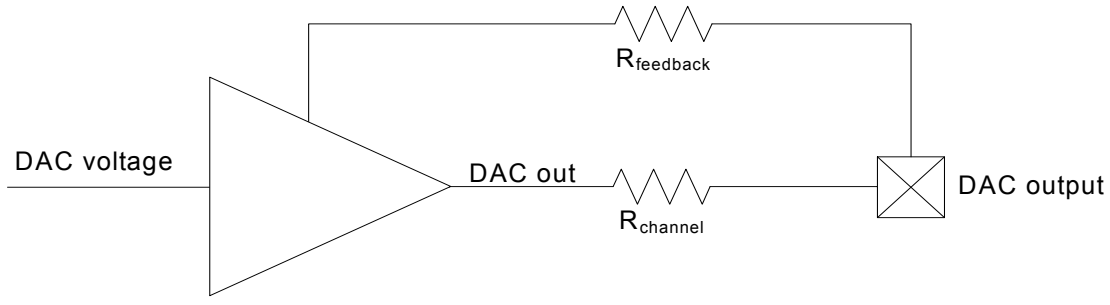
The output voltage from a DAC channel (V_{DAC}) is given as:

$$V_{DACn} = \frac{CHnDATA}{0xFFF} \times VREF$$

29.6 DAC Output model

Each DAC output channel has a driver buffer with feedback to ensure that the voltage on the DAC output pin is equal to the DACs internal voltage. Figure 29-2 on page 368 shows the DAC output model. For details on $R_{channel}$, refer to the DAC characteristics in the device data sheet.

Figure 29-2. DAC output model



29.7 DAC clock

The DAC is clocked directly from the peripheral clock (clk_{PER}), and this puts a limitation on how fast new data can be clocked into the DAC data registers.

29.8 Low Power mode

To reduce the power consumption in DAC conversions, the DAC may be set in a Low Power mode. Conversion time will be longer if new conversions are started in this mode. This increases the DAC conversion time per DAC channel by a factor of two.

29.9 Calibration

For improved accuracy, it is possible to calibrate for gain and offset errors in the DAC.

To get the best calibration result, it is recommended to use the same DAC configuration during calibration as will be used in the final application. The theoretical transfer function for the DAC was shown by the equation in “Output and output channels” on page 368. Including gain and offset errors, the DAC output value can be expressed as:

Equation 29-1. Calculation of DAC output value

$$V_{DAC} = VREF \times \left(\frac{DATA}{0xFFF} \times ERROR_{GAIN}\right) + V_{OFFSET}$$

To calibrate for offset error, output the DAC channel's middle code (0x800) and adjust the offset calibration value until the measured output value is as close as possible to the middle value (VREF / 2). The formula for the offset calibration is given by the Equation 29-2 on page 369, where OCAL is OFFSETCAL and GCAL is GAINCAL.

Equation 29-2. Offset calibration.

$$V_{OCAL} = VREF \times (2 \times OCAL[7] - 1) \times \left(\frac{OCAL[6]}{64} + \frac{OCAL[5]}{128} + \frac{OCAL[4]}{256} + \frac{OCAL[3]}{512} + \frac{OCAL[2]}{1024} + \frac{OCAL[1]}{2048} + \frac{OCAL[0]}{4096}\right)$$

To calibrate for gain error, output the DAC channel's maximum code (0xFFF) and adjust the gain calibration value until the measured output value is as close as possible to the top value (VREF x 4095 / 4096). The gain calibration controls the slope of the DAC characteristic by rotating the transfer function around the middle code. The formula for gain calibration is given by the Equation 29-3 on page 369.

Equation 29-3. Gain calibration.

$$V_{GCAL} = \left(V_{DAC} - \left(\frac{VREF}{2}\right)\right) \times (1 - 2 \times GCAL[7]) \times \left(\frac{GCAL[6]}{16} + \frac{GCAL[5]}{32} + \frac{GCAL[4]}{64} + \frac{GCAL[3]}{128} + \frac{GCAL[2]}{256} + \frac{GCAL[1]}{512} + \frac{GCAL[0]}{1024}\right)$$

Including calibration in the equation, the DAC output can be expressed by Equation 29-4 on page 369.

Equation 29-4.DAC output calculation

$V_{DAC\_out} = V_{DAC} + V_{OCAL} + V_{GCAL}$

29.10 Register description

29.10.1 CTRLA – Control register A

Bit	7	6	5	4	3	2	1	0
+0x00	–	–	–	IDOEN	CH1EN	CH0EN	LPMODE	ENABLE
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:5 – Reserved**
  These bite are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.
- **Bit 4 – IDOEN: Internal Output Enable**
  Setting this bit will enable the internal DAC channel 0 output to be used by the Analog Comparator and ADC. This will then also disable the output pin for DAC Channel 0.
- **Bit 3 – CH1EN: Channel 1 Output Enable**
  Setting this bit will make channel 1 available on the output pin.
- **Bit 2 – CH0EN: Channel 0 Output Enable**
  Setting this bit will make channel 0 available on the output pin unless IDOEN is set to 1.
- **Bit 1 – LPMODE: Low Power Mode**
  Setting this bit enables the DAC low-power mode. The DAC is turned off between each conversion to save current. Conversion time will be doubled when new conversions are started in this mode.
- **Bit 0 – ENABLE: Enable**
  This bit enables the entire DAC.

29.10.2 CTRLB – Control register B

Bit	7	6	5	4	3	2	1	0
+0x01	–	CHSEL[1:0]		–	–	–	CH1TRIG	CH0TRIG
Read/Write	R	R/W	R/W	R	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7 – Reserved**
  This bit is unused and reserved for future use. For compatibility with future devices, always write this bit to zero when this register is written.
- **Bit 6:5 – CHSEL[1:0]: Channel Selection**
  These bits control which DAC channels are enabled and operating. Table 29-1 on page 370 shows the available selections.

Table 29-1. DAC channel selection.

CHSEL[1:0]	Group configuration	Description
00	SINGLE	Single-channel operation on channel 0
01	SINGLE1	Single-channel operation on channel 1
10	DUAL	Dual-channel operation
11	–	Reserved

- **Bit 4:2 – Reserved**
  These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.

- **Bit 1 – CH1TRIG: Auto trigged mode Channel 1**
  If this bit is set, an event on the configured event channel, set in EVCTRL, will trigger a conversion on DAC channel 1 if its data register, CH1DATA, has been updated.

- **Bit 0 – CH0TRIG: Auto trigged mode Channel 0**
  If this bit is set, an event on the configured event channel, set in EVCTRL, will trigger a conversion on DAC channel 0 if its data register, CH0DATA, has been updated.

29.10.3 CTRLC – Control register C

Bit	7	6	5	4	3	2	1	0
+0x02	–	–	–	REFSEL[1:0]		–	–	LEFTADJ
Read/Write	R	R	R	R/W	R/W	R	R	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:5 – Reserved**
  These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.

- **Bit 4:3 – REFSEL[1:0]: Reference Selection**
  These bits select the reference voltage for the DAC according to Table 29-2 on page 371.

Table 29-2. DAC reference selection.

CHSEL[1:0]	Group configuration	Description
00	INT1V	Internal 1.00V
01	AVCC	AV_{CC}
10	AREFA	AREF on PORTA
11	AREFB	AREF on PORTB

- **Bit 2:1 – Reserved**
  These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.

- **Bit 0 - LEFTADJ: Left-Adjust Value**
  If this bit is set, CH0DATA and CH1DATA are left-adjusted.

29.10.4 EVCTRL – Event Control register

Bit	7	6	5	4	3	2	1	0
+0x03	–	–	–	–	EVSEL[3:0]			
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:4 – Reserved**
  These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.

- **Bit 3 – EVSEL[3]: Event Selection bit 3**
  Setting this bit to 1 enables event channel EVSEL[2:0]+1 as the trigger source for DAC Channel 1. When this bit is 0, the same event channel is used as the trigger source for both DAC channels.

- **Bit 2:0 – EVSEL[2:0]: Event Channel Input Selection**
  These bits select which Event System channel is used for triggering a DAC conversion. Table 29-3 on page 372 shows the available selections.

Table 29-3. DAC reference selection.

EVSEL[2:0]	Group configuration	Description
000	0	Event channel 0 as input to DAC
001	1	Event channel 1 as input to DAC
010	2	Event channel 2 as input to DAC
011	3	Event channel 3 as input to DAC
100	4	Event channel 4 as input to DAC
101	5	Event channel 5 as input to DAC
110	6	Event channel 6 as input to DAC
111	7	Event channel 7 as input to DAC

29.10.5 STATUS – Status register

Bit	7	6	5	4	3	2	1	0
+0x05	–	–	–	–	–	–	CH1DRE	CH0DRE
Read/Write	R	R	R	R	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:2 – Reserved**
  These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.

- **Bit 1 – CH1DRE: Channel 1 Data Register Empty**
  This bit when set indicates that the data register for channel 1 is empty, meaning that a new conversion value may be written. Writing to the data register when this bit is cleared will cause the pending conversion data to be over-written. This bit is directly used for DMA requests.

- **Bit 0 – CH0DRE: Channel 0 Data register Empty**
  This bit when set indicates that the data register for channel 0 is empty, meaning that a new conversion value may be written. Writing to the data register when this bit is cleared will cause the pending conversion data to be over-written. This bit is directly used for DMA requests.

29.10.6 CH0DATAH – Channel 0 Data register High

These two channel data registers, CHnDATAH and CHnDATAL, are the high byte and low byte, respectively, of the 12-bit CHnDATA value that is converted to a voltage on DAC channel n. By default, the 12 bits are distributed with 8 bits in CHnDATAL and 4 bits in the four lsb positions of CHnDATAH (right-adjusted).To select left-adjusted data, set the LEFTADJ bit in the CTRLC register.

When left adjusted data is selected, it is possible to do 8-bit conversions by writing only to the high byte of CHnDATA, i.e., CHnDATAH. The TEMP register should be initialized to zero if only 8-bit conversion mode is used.

	Bit	7	6	5	4	3	2	1	0
Right-adjust	+0x19	–	–	–	–	CHDATA[11:8]			
Left-adjust		CHDATA[11:4]							
Right-adjust	Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Left-adjust	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Right-adjust	Initial Value	0	0	0	0	0	0	0	0
Left-adjust	Initial Value	0	0	0	0	0	0	0	0

29.10.6.1 Right-adjusted

- **Bit 7:4 – Reserved**
  These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.

- **Bit 3:0 – CHDATA[11:8]: Conversion Data Channel 0, Four msbs**
  These bits are the four msbs of the 12-bit value to convert to channel 0 in right-adjusted mode.

29.10.6.2 Left-adjusted

- **Bits 7:0 – CHDATA[11:4]: Conversion Data Channel 0, Eight msbs**
  These bits are the eight msbs of the 12-bit value to convert to channel 0 in left-adjusted mode

29.10.7 CH0DATAL – Channel 0 Data register Low

	Bit	7	6	5	4	3	2	1	0
Right-adjust	+0x18	CHDATA[7:0]							
Left-adjust		CHDATA[3:0]				–	–	–	–
Right-adjust	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Left-adjust	Read/Write	R/W	R/W	R/W	R/W	R	R	R	R
Right-adjust	Initial Value	0	0	0	0	0	0	0	0
Left-adjust	Initial Value	0	0	0	0	0	0	0	0

29.10.7.1 Right-adjusted

- **Bit 7:0 – CHDATA[7:0]: Conversion Data Channel 0, Eight lsbs**
  These bits are the eight lsbs of the 12-bit value to convert to channel 0 in right-adjusted mode.

29.10.7.2 Left-adjusted

- **Bit 7:4 – CHDATA[3:0]: Conversion Data Channel 0, Four lsbs**
  These bits are the four lsbs of the 12-bit value to convert to channel 0 in left-adjusted mode.

- **Bit 3:0 – Reserved**
  These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.

29.10.8 CH1DATAH – Channel 1 Data register High

	Bit	7	6	5	4	3	2	1	0
Right-adjust	+0x1B	–	–	–	–	CHDATA[11:8]			
Left-adjust		CHDATA[11:4]							
Right-adjust	Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Left-adjust	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Right-adjust	Initial Value	0	0	0	0	0	0	0	0
Left-adjust	Initial Value	0	0	0	0	0	0	0	0

29.10.8.1 Right-adjusted

- **Bit 7:4 – Reserved**
  These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.
- **Bit 3:0 – CHDATA[11:8]: Conversion Data Channel 1, Four msbs**
  These bits are the four msbs of the 12-bit value to convert to channel 1 in right-adjusted mode.

29.10.8.2 Left-adjusted

- **Bit 7:0 – CHDATA[11:4]: Conversion Data Channel 1, Eight msbs**
  These bits are the eight msbs of the 12-bit value to convert to channel 1 in left-adjusted mode.

29.10.9 CH1DATAL – Channel 1 Data register Low

	Bit	7	6	5	4	3	2	1	0
Right-adjust	+0x1A	CHDATA[7:0]							
Left-adjust		CHDATA[3:0]				–	–	–	–
Right-adjust	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Left-adjust	Read/Write	R/W	R/W	R/W	R/W	R	R	R	R
Right-adjust	Initial Value	0	0	0	0	0	0	0	0
Left-adjust	Initial Value	0	0	0	0	0	0	0	0

29.10.9.1Right-adjusted

- **Bit 7:0 – CHDATA[7:0]: Conversion Data Channel 1, Eight lsbs**
  These bits are the eight lsbs of the 12-bit value to convert to channel 1 in right-adjusted mode.

29.10.9.2 Left-adjusted

- **Bits 7:4 – CHDATA[3:0]: Conversion Data Channel 1, Four lsbs**
  These bits are the four lsbs of the 12-bit value to convert to channel 1 in left-adjusted mode.
- **Bit 3:0 – Reserved**
  These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.

29.10.10 CH0GAINCAL – Gain Calibration register

Bit	7	6	5	4	3	2	1	0
+0x08/+0x0A	CH0GAINCAL[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:0 – CH0GAINCAL[7:0]: Gain Calibration value**
  These bits are used to compensate for the gain error in DAC channel 0. See “Calibration” on page 369 for details.

29.10.11 CH0OFFSETCAL – Offset Calibration register

Bit	7	6	5	4	3	2	1	0
+0x09	CH0OFFSETCAL[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:0 – CH0OFFSETCAL[7:0]: Offset Calibration value**
  These bits are used to compensate for the offset error in DAC channel 0. See “Calibration” on page 369 for details.

29.10.12 CH1GAINCAL – Gain Calibration register

Bit	7	6	5	4	3	2	1	0
+0x0A	CH1GAINCAL[7:0]							
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:0 – CH1GAINCAL[7:0]: Gain Calibration value**
  These bits are used to compensate for the gain error in DAC channel 1. See “Calibration” on page 369 for details.

29.10.13 CH1OFFSETCAL – Offset Calibration register

Bit	7	6	5	4	3	2	1	0
+0x0B	CH1OFFSETCAL[7:0]							
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:0 – CH1OFFSETCAL[7:0]: Offset Calibration value**
  These bits are used to compensate for the offset error in DAC channel 1. See “Calibration” on page 369 for details.

29.11 Register summary

This is the I/O summary when the DAC is configured to give standard 12-bit results. The I/O summary for 12-bit left-adjusted results will be similar, but with some changes in the CHnDATAL and CHnDATAH data registers.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
+0x00	CTRLA	–	–	–	IDOEN	CH1EN	CH0EN	LPMODE	ENABLE	370
+0x01	CTRLB	–	CHSEL[1:0]		–	–	–	CH1TRIG	CH0TRIG	370
+0x02	CTRLC	–	–	–	REFSEL[1:0]		–	–	LEFTADJ	371
+0x03	EVCTRL	–	–	–	–	EVSEL[3:0]				371
+0x04	Reserved	–	–	–	–	–	–	–	–	
+0x05	STATUS	–	–	–	–	–	–	CH1DRE	CH0DRE	372
+0x06	Reserved	–	–	–	–	–	–	–	–	
+0x07	Reserved	–	–	–	–	–	–	–	–	
+0x08	CH0GAINCAL	CH0GAINCAL[7:0]								374
+0x09	CH0OFFSETCAL	CH0OFFSETCAL[7:0]								375
+0x0A	CH1GAINCAL	CH1GAINCAL[7:0]								375
+0x0B	CH1OFFSETCAL	CH1OFFSETCAL[7:0]								375
+0x12	Reserved	–	–	–	–	–	–	–	–	
+0x13	Reserved	–	–	–	–	–	–	–	–	
+0x14	Reserved	–	–	–	–	–	–	–	–	
+0x15	Reserved	–	–	–	–	–	–	–	–	
+0x16	Reserved	–	–	–	–	–	–	–	–	
+0x17	Reserved	–	–	–	–	–	–	–	–	
+0x18	CH0DATAL	CHDATA[7:0]								373
+0x19	CH0DATAH	–	–	–	–	CHDATA[11:8]				372
+0x1A	CH1DATAL	CHDATA[7:0]								374
+0x1B	CH1DATAH	–	–	–	–	CHDATA[11:8]				374