9. Reset System

9.1 Features

- Reset the microcontroller and set it to initial state when a reset source goes active
- Multiple reset sources that cover different situations
  - Power-on reset
  - External reset
  - Watchdog reset
  - Brownout reset
  - PDI reset
  - Software reset
- Asynchronous operation
  - No running system clock in the device is required for reset
- Reset status register for reading the reset source from the application code

9.2 Overview

The reset system issues a microcontroller reset and sets the device to its initial state. This is for situations where operation should not start or continue, such as when the microcontrollers operates below its power supply rating. If a reset source goes active, the device enters and is kept in reset until all reset sources have released their reset. The I/O pins are immediately tri-stated. The program counter is set to the reset vector location, and all I/O registers are set to their initial values. The SRAM content is kept. However, if the device accesses the SRAM when a reset occurs, the content of the accessed location can not be guaranteed.

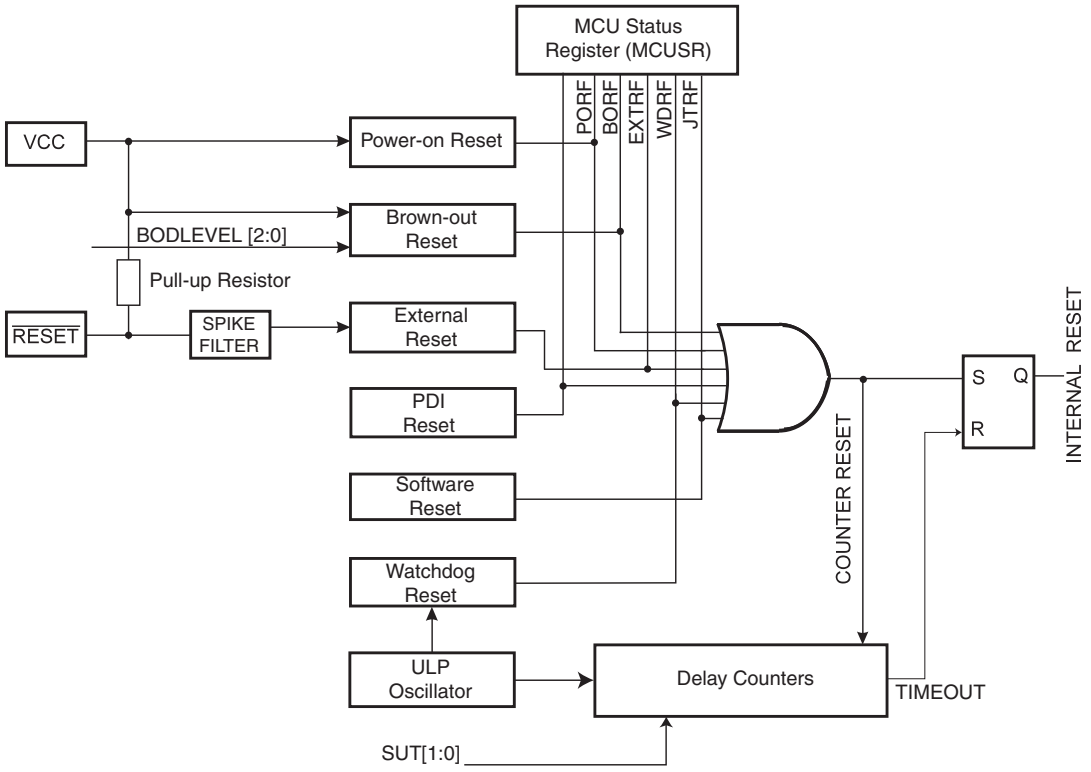
After reset is released from all reset sources, the default oscillator is started and calibrated before the device starts running from the reset vector address. By default, this is the lowest program memory address, 0, but it is possible to move the reset vector to the lowest address in the boot section.

The reset functionality is asynchronous, and so no running system clock is required to reset the device. The software reset feature makes it possible to issue a controlled system reset from the user software.

The reset status register has individual status flags for each reset source. It is cleared at power-on reset, and shows which sources have issued a reset since the last power-on.

An overview of the reset system is shown in Figure 9-1 on page 111.

Figure 9-1. Reset system overview.



9.3 Reset Sequence

A reset request from any reset source will immediately reset the device and keep it in reset as long as the request is active. When all reset requests are released, the device will go through three stages before the device starts running again:

- Reset counter delay
- Oscillator startup
- Oscillator calibration

If another reset requests occurs during this process, the reset sequence will start over again.

9.3.1 Reset Counter

The reset counter can delay reset release with a programmable period from when all reset requests are released. The reset delay is timed from the 1kHz output of the ultra low power (ULP) internal oscillator, and in addition 24 System clock (clk_{SYS}) cycles are counted before reset is released. The reset delay is set by the STARTUPTIME fuse bits. The selectable delays are shown in Table 9-1 on page 111.

Table 9-1. Reset delay.

SUT[1:0]	Number of 1kHz ULP Oscillator Clock Cycles	Recommended Usage
00	64 Clk_{ULP}+ 24 Clk_{SYS}	Stable frequency at startup
01	4 Clk_{ULP} + 24 Clk_{SYS}	Slowly rising power
10	Reserved	–
11	24 Clk_{SYS}	Fast rising power or BOD enabled

Whenever a reset occurs, the clock system is reset and the internal 2MHz internal oscillator is chosen as the source for Clk_{SYS}.

9.3.2 Oscillator Startup

After the reset delay, the 2MHz internal oscillator clock is started, and its calibration values are automatically loaded from the calibration row to the calibration registers.

9.4 Reset Sources

9.4.1 Power-on Reset

A power-on reset (POR) is generated by an on-chip detection circuit. The POR is activated when the V_{CC} rises and reaches the POR threshold voltage (V_{POT}), and this will start the reset sequence.

The POR is also activated to power down the device properly when the V_{CC} falls and drops below the V_{POT} level.

The V_{POT} level is higher for falling V_{CC}than for rising V_{CC}. Consult the datasheet for POR characteristics data.

Figure 9-2. MCU startup, $\overline{\textbf{RESET}}$ tied to V_{CC}.

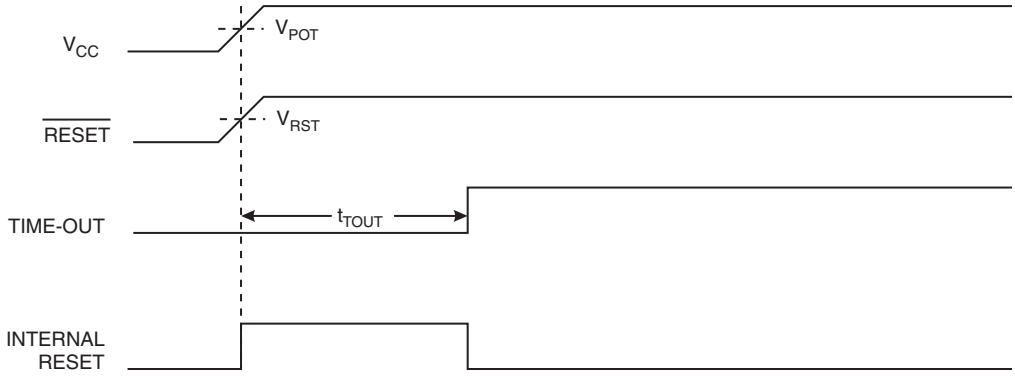
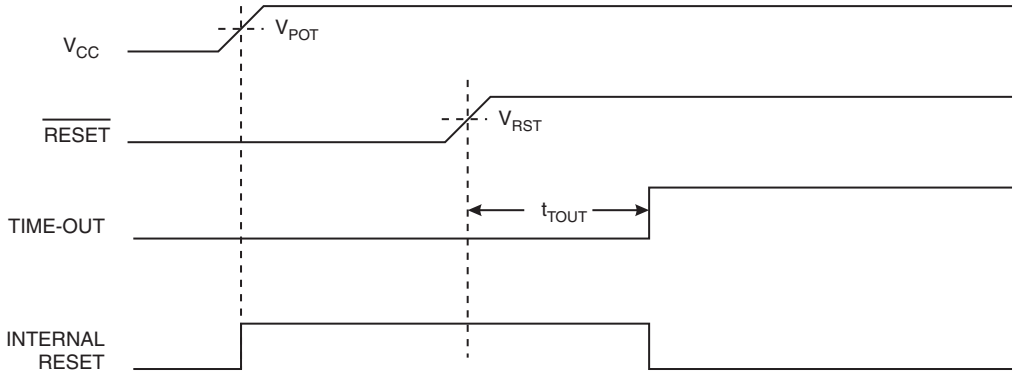


Figure 9-3. MCU startup, $\overline{\textbf{RESET}}$ extended externally,



9.4.2 Brownout Detection

The on-chip brownout detection (BOD) circuit monitors the V_{CC} level during operation by comparing it to a fixed, programmable level that is selected by the BODLEVEL fuses. If disabled, BOD is forced on at the lowest level during chip erase and when the PDI is enabled.

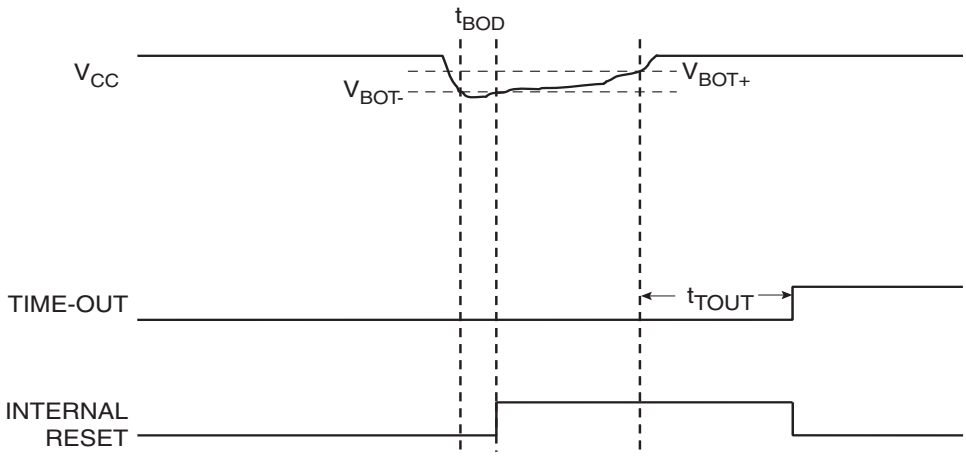
When the BOD is enabled and V_{CC} decreases to a value below the trigger level (V_{BOT-} in Figure 9-4), the brownout reset is immediately activated.

When V_{CC} increases above the trigger level (V_{BOT+} in Figure 9-4), the reset counter starts the MCU after the timeout period, t_{TOUT}, has expired.

The trigger level has a hysteresis to ensure spike free brownout detection. The hysteresis on the detection level should be interpreted as $V_{BOT+} = V_{BOT} + V_{HYST}/2$ and $V_{BOT-} = V_{BOT} - V_{HYST}/2$.

The BOD circuit will detect a drop in V_{CC} only if the voltage stays below the trigger level for longer than t_{BOD}.

Figure 9-4. Brownout detection reset.



For BOD characterization data consult the device datasheet. The programmable BODLEVEL setting is shown in Table 9-2 on page 113.

Table 9-2. Programmable BODLEVEL setting.

BOD level	Fuse BODLEVEL[2:0](2)	V_{BOT}(1)	Unit
BOD level 0	111	1.6	V
BOD level 1	110	1.8	
BOD level 2	101	2.0	
BOD level 3	100	2.2	
BOD level 4	011	2.4	
BOD level 5	010	2.6	
BOD level 6	001	2.8	
BOD level 7	000	3.0	

Notes: 1. The values are nominal values only. For accurate, actual numbers, consult the device datasheet.
2. Changing these fuse bits will have no effect until leaving programming mode.

The BOD circuit has three modes of operation:

- **Disabled:** In this mode, there is no monitoring of the V_{CC} level.
- **Enabled:** In this mode, the V_{CC} level is continuously monitored, and a drop in V_{CC} below V_{BOT} for a period of t_{BOD} will give a brownout reset
- **Sampled:** In this mode, the BOD circuit will sample the V_{CC} level with a period identical to that of the 1kHz output from the ultra low power (ULP) internal oscillator. Between each sample, the BOD is turned off. This mode will

reduce the power consumption compared to the enabled mode, but a fall in the V_{CC} level between two positive edges of the 1kHz ULP oscillator output will not be detected. If a brownout is detected in this mode, the BOD circuit is set in enabled mode to ensure that the device is kept in reset until V_{CC} is above V_{BOT} again

The BODACT fuse determines the BOD setting for active mode and idle mode, while the BODPD fuse determines the brownout detection setting for all sleep modes, except idle mode.

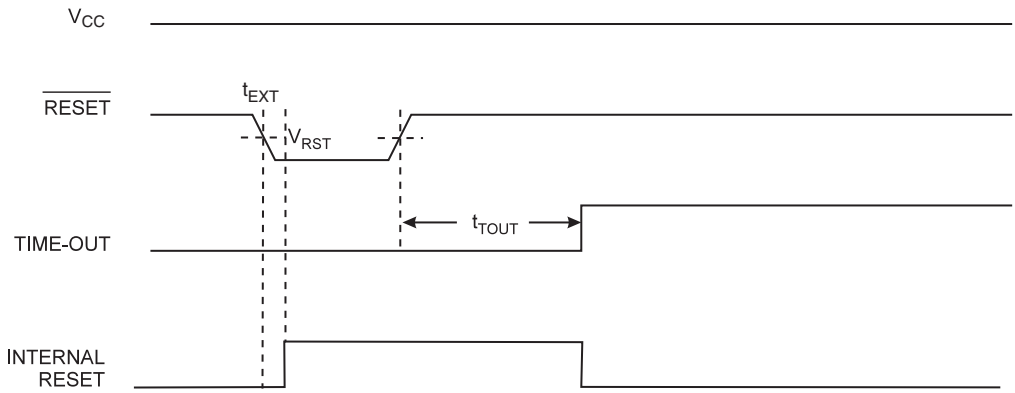
Table 9-3. BOD setting fuse decoding.

BODACT[1:0]/ BODPD[1:0]	Mode
00	Reserved
01	Sampled
10	Enabled
11	Disabled

9.4.3 External Reset

The external reset circuit is connected to the external $\overline{\text{RESET}}$ pin. The external reset will trigger when the $\overline{\text{RESET}}$ pin is driven below the $\overline{\text{RESET}}$ pin threshold voltage, V_{RST}, for longer than the minimum pulse period, t_{EXT}. The reset will be held as long as the pin is kept low. The $\overline{\text{RESET}}$ pin includes an internal pull-up resistor.

Figure 9-5. External reset characteristics.

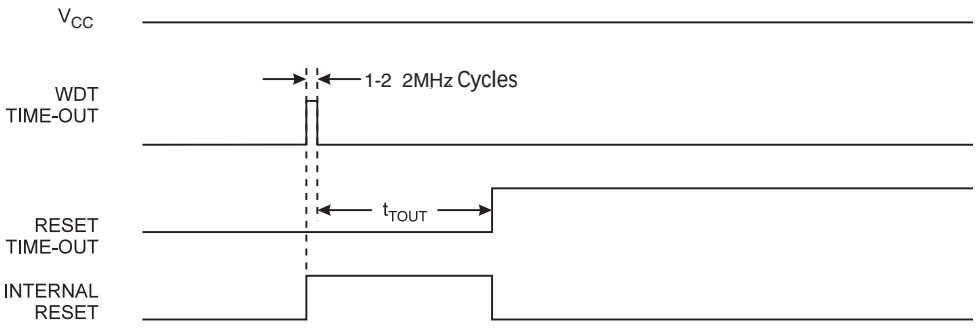


For external reset characterization data consult the device datasheet.

9.4.4 Watchdog Reset

The watchdog timer (WDT) is a system function for monitoring correct program operation. If the WDT is not reset from the software within a programmable timout period, a watchdog reset will be given. The watchdog reset is active for one to two clock cycles of the 2MHz internal oscillator.

Figure 9-6. Watchdog reset.

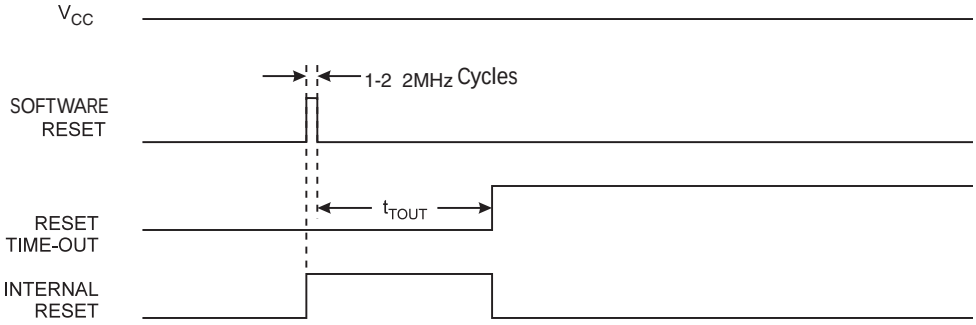


For information on configuration and use of the WDT, refer to the "WDT – Watchdog Timer" on page 125.

9.4.5 Software Reset

The software reset makes it possible to issue a system reset from software by writing to the software reset bit in the reset control register.The reset will be issued within two CPU clock cycles after writing the bit. It is not possible to execute any instruction from when a software reset is requested until it is issued.

Figure 9-7. Software reset.



9.4.6 Program and Debug Interface Reset

The program and debug interface reset contains a separate reset source that is used to reset the device during external programming and debugging. This reset source is accessible only from external debuggers and programmers.

9.5 Register Description

9.5.1 STATUS – Status register

Bit	7	6	5	4	3	2	1	0
+0x00	–	–	SRF	PDIRF	WDRF	BORF	EXTRF	PORF
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	–	–	–	–	–	–	–	–

- **Bit 7:6 – Reserved**
  These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.
- **Bit 5 – SRF: Software Reset Flag**
  This flag is set if a software reset occurs. The flag will be cleared by a power-on reset or by writing a one to the bit location.
- **Bit 4 – PDIRF: Program and Debug Interface Reset Flag**
  This flag is set if a programming interface reset occurs. The flag will be cleared by a power-on reset or by writing a one to the bit location.
- **Bit 3 – WDRF: Watchdog Reset Flag**
  This flag is set if a watchdog reset occurs. The flag will be cleared by a power-on reset or by writing a one to the bit location.
- **Bit 2 – BORF: Brownout Reset Flag**
  This flag is set if a brownout reset occurs. The flag will be cleared by a power-on reset or by writing a one to the bit location.
- **Bit 1 – EXTRF: External Reset Flag**
  This flag is set if an external reset occurs. The flag will be cleared by a power-on reset or by writing a one to the bit location.
- **Bit 0 – PORF: Power On Reset Flag**
  This flag is set if a power-on reset occurs. Writing a one to the flag will clear the bit location.

9.5.2 CTRL – Control register

Bit	7	6	5	4	3	2	1	0
+0x01	–	–	–	–	–	–	–	SWRST
Read/Write	R	R	R	R	R	R	R	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:1 – Reserved**
  These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.
- **Bit 0 – SWRST: Software Reset**
  When this bit is set, a software reset will occur. The bit is cleared when a reset is issued. This bit is protected by the configuration change protection mechanism. For details, refer to “Configuration Change Protection” on page 13.

9.6 Register summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	bit 0	Page
+0x00	STATUS	–	–	SRF	PDIRF	WDRF	BORF	EXTRF	PORF	116
+0x01	CTRL	–	–	–	–	–	–	–	SWRST	116