15. TC2 – 16-bit Timer/Counter Type 2

15.1 Features

- A system of two eight-bit timer/counters
  - Low-byte timer/counter
  - High-byte timer/counter
- Eight compare channels
  - Four compare channels for the low-byte timer/counter
  - Four compare channels for the high-byte timer/counter
- Waveform generation
  - Single slope pulse width modulation
- Timer underflow interrupts/events
- One compare match interrupt/event per compare channel for the low-byte timer/counter
- Can be used with the event system for count control
- Can be used to trigger DMA transactions

15.2 Overview

A timer/counter 2 is realized when a timer/counter 0 is set in split mode. It is a system of two eight-bit timer/counters, each with four compare channels. This results in eight configurable pulse width modulation (PWM) channels with individually controlled duty cycles, and is intended for applications that require a high number of PWM channels.

The two eight-bit timer/counters in this system are referred to as the low-byte timer/counter and high-byte timer/counter, respectively. The difference between them is that only the low-byte timer/counter can be used to generate compare match interrupts, events and DMA triggers.

The two eight-bit timer/counters have a shared clock source and separate period and compare settings. They can be clocked and timed from the peripheral clock, with optional prescaling, or from the event system. The counters are always counting down.

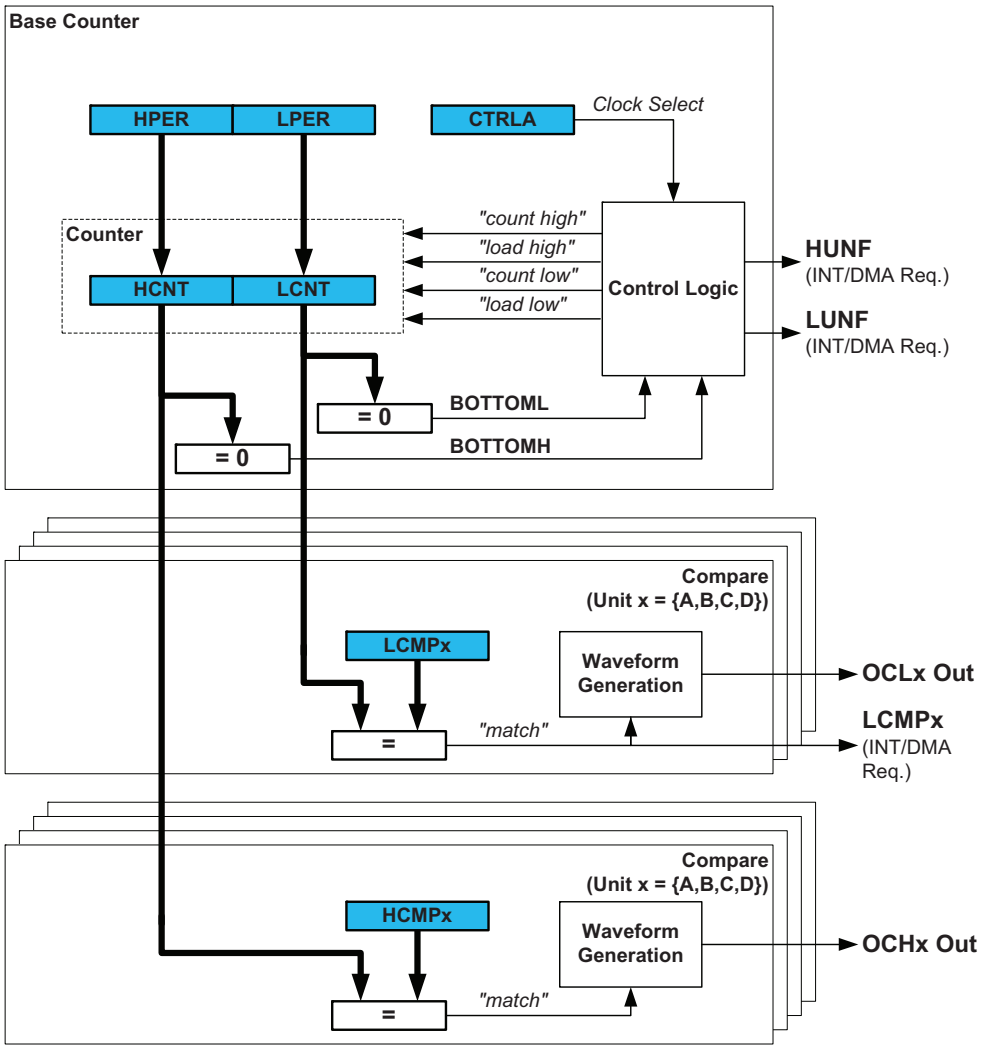
The high resolution (hi-res) extension can be used to increase the waveform output resolution by up to eight times by using an internal clock source running up to four times faster than the peripheral clock.

The timer/counter 2 is set back to timer/counter 0 by setting it in normal mode; hence, one timer/counter can exist only as either type 0 or type 2.

A detailed block diagram of the timer/counter 2 showing the low-byte (L) and high-byte (H) timer/counter register split and compare modules is shown in Figure 15-1 on page 187.

15.3 Block Diagram

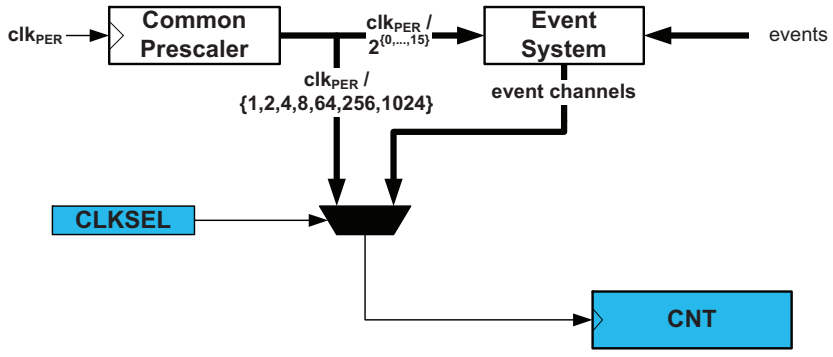
Figure 15-1. Block diagram of the 16-bit timer/counter 0 with split mode.



15.4 Clock Sources

The timer/counter can be clocked from the peripheral clock (clk_{PER}) and from the event system. Figure 15-2 shows the clock and event selection.

Figure 15-2. Clock selection.



The peripheral clock (clk_{PER}) is fed into the common prescaler (common for all timer/counters in a device). A selection of prescaler outputs from 1 to 1/1024 is directly available. In addition, the whole range of time prescalings from 1 to 2^{15} is available through the event system.

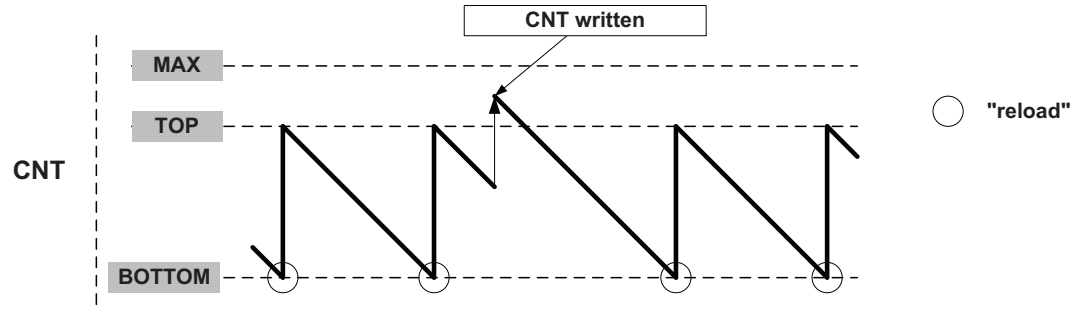
The clock selection (CLKSEL) selects one of the clock prescaler outputs or an event channel for the high-byte counter (HCNT) and low-byte counter (LCNT). By using the event system, any event source, such as an external clock signal, on any I/O pin can be used as the clock input.

By default, no clock input is selected, and the counters are not running.

15.5 Counter Operation

The counters will always count in single-slope mode. Each counter counts down for each clock cycle until it reaches BOTTOM, and then reloads the counter with the period register value at the following clock cycle.

Figure 15-3. Counter operation.

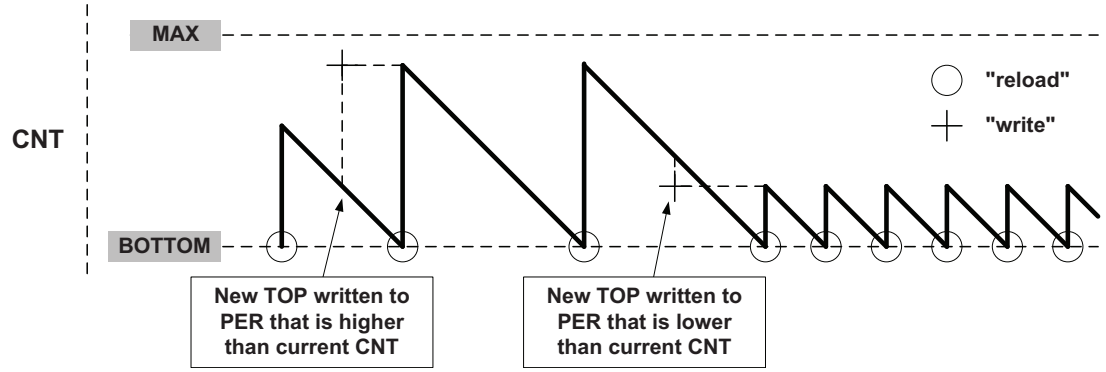


As shown in Figure 15-3, the counter can change the counter value while running. The write access has higher priority than the count clear, and reloads and will be immediate.

15.5.1 Changing the Period

The counter period is changed by writing a new TOP value to the period register. Since the counter is counting down, the period register can be written at any time without affecting the current period, as shown in Figure 15-4 on page 188. This prevents wraparound and generation of odd waveforms.

Figure 15-4. Changing the period.



15.6 Compare Channel

Each compare channel continuously compares the counter value with the CMPx register. If CNT equals CMPx, the comparator signals a match. For the low-byte timer/counter, the match will set the compare channel's interrupt flag at the next timer clock cycle, and the event and optional interrupt is generated. The high-byte timer/counter does not have compare interrupt/event.

15.6.1 Waveform Generation

The compare channels can be used for waveform generation on the corresponding port pins. To make the waveform visible on the connected port pin, the following requirements must be fulfilled:

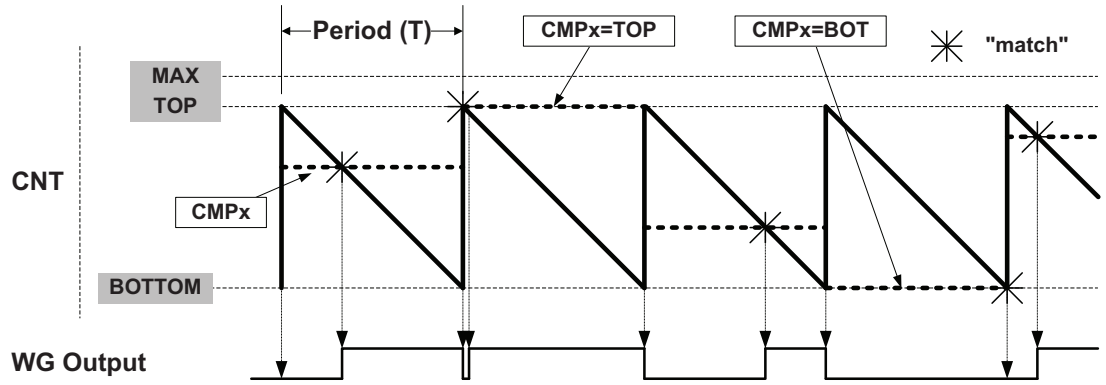
1. The compare channels to be used must be enabled. This will override the corresponding port pin output register.
2. The direction for the associated port pin must be set to output.

Inverted waveform output can be achieved by setting invert I/O on the port pin. Refer to "I/O Ports" on page 139 for more details.

15.6.2 Single-slope PWM Generation

For PWM generation, the period (T) is controlled by the PER register, while the CMPx registers control the duty cycle of the waveform generator (WG) output. Figure 15-5 on page 189 shows how the counter counts from TOP to BOTTOM, and then restarts from TOP. The WG output is set on the compare match between the CNT and CMPx registers, and cleared at BOTTOM.

Figure 15-5. Single-slope pulse width modulation.



The PER register defines the PWM resolution. The minimum resolution is two bits (PER=0x0003), and the maximum resolution is eight bits (PER=MAX).

The following equation is used to calculate the exact resolution for a single-slope PWM (R_{PWM_SS}) waveform:

$$R_{PWM\_SS} = \frac{\log(PER + 1)}{\log(2)}$$

The single, slow PWM frequency (f_{PWM_SS}) depends on the period setting (PER) and the peripheral clock frequency (f_{PER}), and it is calculated by using the following equation:

$$f_{PWM\_SS} = \frac{f_{PER}}{N(PER + 1)}$$

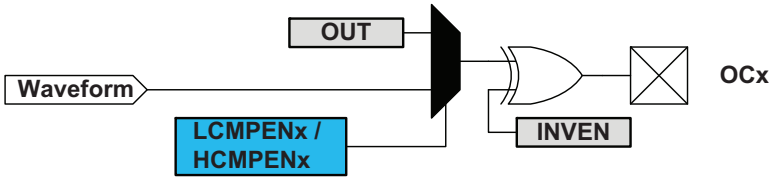
where N represents the prescaler divider used (1, 2, 4, 8, 64, 256, 1024, or event channel n).

15.6.3 Port Override for Waveform Generation

To make the waveform generation available on the port pins, the corresponding port pin direction must be set as output. The timer/counter will override the port pin values when the CMP channel is enabled (LCMPENx/HCMPENx).

Figure 15-6 on page 190 shows the port override for the low- and high-byte timer/counters. For the low-byte timer/counter, CMP channels A to D will override the output value (OUTxn) of port pins 0 to 3 on the corresponding port pins (Pxn). For the high-byte timer/counter, CMP channels E to H will override port pins 4 to 7. Enabling inverted I/O on the port pin (INVENxn) inverts the corresponding WG output.

Figure 15-6. Port override for low- and high-byte timer/counters.



15.7 Interrupts and Events

The timer/counters can generate interrupts and events. The counter can generate an interrupt on underflow, and each CMP channel for the low-byte counter has a separate compare interrupt.

Events will be generated for all conditions that can generate interrupts. For details on event generation and available events, refer to “Event System” on page 70.

15.8 DMA Support

Timer/counter underflow and compare interrupt flags can trigger a DMA transaction. The acknowledge condition that clears the flag/request is listed in Table 15-1 on page 190.

Table 15-1. DMA request sources.

Request	Acknowledge	Comment
LUNFIF	DMAC writes to LCNT DMAC writes to LPER	
HUNFIF	DMAC writes to HCNT DMAC writes to HPER	
CCIF{D,C,B,A}	DMAC access of LCMP{D,C,B,A}	Output compare operation

15.9 Timer/Counter Commands

A set of commands can be given to the timer/counter by software to immediately change the state of the module. These commands give direct control of the update, restart, and reset signals.

The software can force a restart of the current waveform period by issuing a restart command. In this case the counter, direction, and all compare outputs are set to zero.

A reset command will set all timer/counter registers to their initial values. A reset can only be given when the timer/counter is not running (OFF).

15.10 Register description

15.10.1 CTRLA – Control register A

Bit	7	6	5	4	3	2	1	0
+0x00	–	–	–	–	CLKSEL[3:0]			
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:4 – Reserved**
  These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.

- **Bit 3:0 – CLKSEL[3:0]: Clock Select**
  These bits select clock source for the timer/counter according to Table 15-2 on page 191. The clock select is identical for both high- and low-byte timer/counters.

Table 15-2. Clock select.

CLKSEL[3:0]	Group configuration	Description
0000	OFF	None (i.e., timer/counter in OFF state)
0001	DIV1	Prescaler: Clk_{PER}
0010	DIV2	Prescaler: $Clk_{PER}/2$
0011	DIV4	Prescaler: $Clk_{PER}/4$
0100	DIV8	Prescaler: $Clk_{PER}/8$
0101	DIV64	Prescaler: $Clk_{PER}/64$
0110	DIV256	Prescaler: $Clk_{PER}/256$
0111	DIV1024	Prescaler: $Clk_{PER}/1024$
1nnn	EVCHn	Event channel n, n= [0,...,7]

15.10.2 CTRLB – Control register B

Bit	7	6	5	4	3	2	1	0
+0x01	HCMPEND	HCMPENC	HCMPENB	HCMPENA	LCMPEND	LCMPENC	LCMPENB	LCMPENA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:0 – HCMPENx / LCMPENx: High/Low Byte Compare Enable x**
  Setting these bits will enable the compare output and override the port output register for the corresponding OCn output pin.

15.10.3 CTRLC – Control register C

Bit	7	6	5	4	3	2	1	0
+0x02	HCMPD	HCMPC	HCMPB	HCMPA	LCMPD	LCMPC	LCMPB	LCMPA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:0 – HCMPx/LCMPx: High/Low Compare x Output Value**
  These bits allow direct access to the waveform generator's output compare value when the timer/counter is OFF. This is used to set or clear the WG output value when the timer/counter is not running.

15.10.4 CTRLE – Control register E

Bit	7	6	5	4	3	2	1	0
+0x04	–	–	–	–	–	–	BYTEM[1:0]	
Read/Write	R	R	R	R	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:2 – Reserved**
  These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.
- **Bit 1:0 – BYTEM[1:0]: Byte Mode**
  These bits select the timer/counter operation mode according to Table 15-3 on page 192.

Table 15-3. Byte mode.

BYTEM[1:0]	Group configuration	Description
00	NORMAL	Timer/counter is set to normal mode (timer/counter type 0)
01	BYTEMODE	Upper byte of the counter (HCNT) will be set to zero after each counter clock.
10	SPLITMODE	Timer/counter is split into two eight-bit timer/counters (timer/counter type 2)
11	–	Reserved

15.10.5 INTCTRLA – Interrupt Enable register A

Bit	7	6	5	4	3	2	1	0
+0x06	–	–	–	–	HUNFINTLVL[1:0]		LUNFINTLVL[1:0]	
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:4 – Reserved**
  These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.
- **Bit 3:2 – HUNFINTLVL[1:0]: High-byte Timer Underflow Interrupt Level**
  These bits enable the high-byte timer underflow interrupt and select the interrupt level, as described in “Interrupts and Programmable Multilevel Interrupt Controller” on page 131. The enabled interrupt will be triggered when HUNFIF in the INTFLAGS register is set.

- **Bit 1:0 – LUNFINTLVL[1:0]: Low-byte Timer Underflow Interrupt Level**
  These bits enable the low-byte timer underflow interrupt and select the interrupt level, as described in “Interrupts and Programmable Multilevel Interrupt Controller” on page 131. The enabled interrupt will be triggered when LUNFIF in the INTFLAGS register is set.

15.10.6 INTCTRLB – Interrupt Enable register B

Bit	7	6	5	4	3	2	1	0
+0x07	LCMPDINTLVL[1:0]		LCMPCINTLVL[1:0]		LCMPBINTLVL[1:0]		LCMPAINTLVL[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:0 – LCMPxINTLVL[1:0]: Low-byte Compare x Interrupt Level**
  These bits enable the low-byte timer compare interrupt and select the interrupt level, as described in “Interrupts and Programmable Multilevel Interrupt Controller” on page 131. The enabled interrupt will be triggered when LCMPxIF in the INTFLAGS register is set.

15.10.7 CTRLF – Control register F

Bit	7	6	5	4	3	2	1	0
+0x08	–	–	–	–	CMD[1:0]		CMDEN[1:0]	
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:4 – Reserved**
  These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.

- **Bit 3:2 – CMD[1:0]: Timer/Counter Command**
  These command bits are used for software control of timer/counter update, restart, and reset. The command bits are always read as zero. The CMD bits must be used together with CMDEN.

Table 15-4. Command selections.

CMD	Group configuration	Description
00	NONE	None
01	–	Reserved
10	RESTART	Force restart
11	RESET	Force hard reset (ignored if T/C is not in OFF state)

- **Bit 1:0 – CMDEN[1:0]: Command Enable**
  These bits are used to indicate for which timer/counter the command (CMD) is valid

Table 15-5. Command selections.

CMD	Group configuration	Description
00	–	Reserved
01	LOW	Command valid for low-byte T/C
10	HIGH	Command valid for high-byte T/C
11	BOTH	Command valid for both low-byte and high-byte T/C

15.10.8 INTFLAGS – Interrupt Flag register

Bit	7	6	5	4	3	2	1	0
+0x0C	LCMPDIF	LCMPCIF	LCMPBIF	LCMPAIF	–	–	HUNFIF	LUNFIF
Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:4 – LCMPxIF: Compare Channel x Interrupt Flag**
  The compare interrupt flag (LCMPxIF) is set on a compare match on the corresponding CMP channel.
  For all modes of operation, LCMPxIF will be set when a compare match occurs between the count register (LCNT) and the corresponding compare register (LCMPx). The LCMPxIF is automatically cleared when the corresponding interrupt vector is executed. The flag can also be cleared by writing a one to its bit location.
- **Bit 3:2 – Reserved**
  These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.
- **Bit 1 – HUNFIF: High-byte Timer Underflow Interrupt Flag**
  HUNFIF is set on a BOTTOM (underflow) condition. This flag is automatically cleared when the corresponding interrupt vector is executed. The flag can also be cleared by writing a one to its bit location.
- **Bit 0 – LUNFIF: Low-byte Timer Underflow Interrupt Flag**
  LUNFIF is set on a BOTTOM (underflow) condition. This flag is automatically cleared when the corresponding interrupt vector is executed. The flag can also be cleared by writing a one to its bit location.

15.10.9 LCNT – Low-byte Count register

Bit	7	6	5	4	3	2	1	0
+0x20	LCNT[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:0 – LCNT[7:0]**
  LCNT contains the eight-bit counter value for the low-byte timer/counter. The CPU and DMA write accesses have priority over count, clear, or reload of the counter.

15.10.10 HCNT – High-byte Count register

Bit	7	6	5	4	3	2	1	0
+0x21	HCNT[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:0 – HCNT[7:0]**
  HCNT contains the eight-bit counter value for the high-byte timer/counter. The CPU and DMA write accesses have priority over count, clear, or reload of the counter.

15.10.11 LPER – Low-byte Period register

Bit	7	6	5	4	3	2	1	0
+0x27	LPER[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:0 – LPER[7:0]**
  LPER contains the eight-bit period value for the low-byte timer/counter.

15.10.12 HPER – High-byte Period register

Bit	7	6	5	4	3	2	1	0
+0x26	HPER[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:0 – HPER[7:0]**
  HPER contains the eight-bit period for the high-byte timer/counter.

15.10.13 LCMPx – Low-byte Compare register x

Bit	7	6	5	4	3	2	1	0
	LCMPx[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:0 – LCMPx[7:0], x =[A, B, C, D]**
  LCMPx contains the eight-bit compare value for the low-byte timer/counter.

  These registers are all continuously compared to the counter value. Normally, the outputs from the comparators are then used for generating waveforms.

15.10.14 HCMPx – High-byte Compare register x

Bit	7	6	5	4	3	2	1	0
	HCMPx[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 7:0 – HCMPx[7:0], x =[A, B, C, D]**
  HCMPx contains the eight-bit compare value for the high-byte timer/counter.
  These registers are all continuously compared to the counter value. Normally the outputs from the comparators are then used for generating waveforms.

15.11 Register summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
+0x00	CTRLA	–	–	–	–	CLKSEL[3:0]				191
+0x01	CTRLB	HCMPDEN	HCMPCEN	HCMPBEN	HCMPAEN	LCMPDEN	LCMPCEN	LCMPBEN	LCMPAEN	191
+0x02	CTRLC	HCMPD	HCMPC	HCMPB	HCMPA	LCMPD	LCMPC	LCMPB	LCMPA	192
+0x05	Reserved									
+0x04	CTRLE							BYTEM[1:0]		192
+0x05	Reserved									
+0x06	INTCTRLA	–	–	–	–	HUNFINTLVL[1:0]		LUNFINTLVL[1:0]		192
+0x07	INTCTRLB	LCMPDINTLVL[1:0]		LCMPCINTLVL[1:0]		LCMPBINTLVL[1:0]		LCMPAINTLVL[1:0]		193
+0x08	Reserved	–	–	–	–	–	–	–	–	
+0x09	CTRLF	–	–	–	–	CMD[1:0]		CMDEN[1:0]		193
+0x0A	Reserved	–	–	–	–	–	–	–	–	
+0x0B	Reserved	–	–	–	–	–	–	–	–	
+0x0C	INTFLAGS	LCMPDIF	LCMPCIF	LCMPBIF	LCMPAIF	–	–	HUNFIF	LUNFIF	194
+0x0D	Reserved	–	–	–	–	–	–	–	–	
+0x0E	Reserved	–	–	–	–	–	–	–	–	
+0x0F	Reserved	–	–	–	–	–	–	–	–	
+0x10 to +0x1F	Reserved	–	–	–	–	–	–	–	–	
+0x20	LCNT	Low-byte Timer/Counter Count Register								195
+0x21	HCNT	High-byte Timer/Counter Count Register								195
+0x22 to +0x25	Reserved	–	–	–	–	–	–	–	–	
+0x26	LPER	Low-byte Timer/Counter Period Register								195
+0x27	HPER	High-byte Timer/Counter Period Register								196
+0x28	LCMPA	Low-byte Compare Register A								195
+0x29	HCMPA	High-byte Compare Register A								196
+0x2A	LCMPB	Low-byte Compare Register B								195
+0x2B	HCMPB	High-byte Compare Register B								196
+0x2C	LCMPC	Low-byte Compare Register C								195
+0x02D	HCMPC	High-byte Compare Register C								196
+0x2E	LCMPD	Low-byte Compare Register D								195
+0x2F	HCMPD	High-byte Compare Register D								196
+0x30 to +0x3F	Reserved	–	–	–	–	–	–	–	–	

15.12 Interrupt vector summary

Table 15-6. Timer/counter interrupt vectors and their word offset addresses.

Offset	Source	Interrupt description
0x00	LUNF_vect	Low-byte Timer/counter underflow interrupt vector offset
0x02	HUNF_vect	High-byte Timer/counter underflow interrupt vector offset
0x4	LCMPA_vect	Low-byte Timer/counter compare channel A interrupt vector offset
0x6	LCMPB_vect	Low-byte Timer/counter compare channel B interrupt vector offset
0x8	LCMPC_vect	Low-byte Timer/counter compare channel C interrupt vector offset
0x0A	LCMPD_vect	Low-byte Timer/counter compare channel D interrupt vector offset