# I/O Pin Characteristics - Absolute Maximums

- Don't operate near the absolute maximums.
- Beyond these points, damage is likely to occur.

### 37.1.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 37-1 on page 74 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 37-1. Absolute maximum ratings.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power supply voltage | | -0.3 | | 4 | V |
| $I_{VCC}$ | Current into a $V_{CC}$ pin | | | | 200 | mA |
| $I_{GND}$ | Current out of a Gnd pin | | | | 200 | |
| $V_{PIN}$ | Pin voltage with respect to Gnd and $V_{CC}$ | | -0.5 | | $V_{CC}$+0.5 | V |
| $I_{PIN}$ | I/O pin sink/source current | | -25 | | 25 | mA |
| $T_A$ | Storage temperature | | -65 | | 150 | °C |
| $T_j$ | Junction temperature | | | | 150 | |

Figure 1: Absolute Ratings

# I/O Pin Characteristics - General Operating Specifications

- For specifications be met (electrical and timing), these must be obeyed.

**37.1.2 General Operating Ratings**

The device must operate within the ratings listed in Table 37-2 in order for all other electrical characteristics and typical characteristics of the device to be valid.

**Table 37-2. General operating conditions.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power supply voltage | | 1.60 | | 3.6 | V |
| $AV_{CC}$ | Analog supply voltage | | 1.60 | | 3.6 | |
| $T_A$ | Temperature range | | -40 | | 85 | °C |
| $T_j$ | Junction temperature | | -40 | | 105 | |

Figure 2: General Operating Conditions

# I/O Pin Characteristics - Pin Specifications

**Table 37-7. I/O pin characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{OH}$ (1)/ $I_{OL}$ (2) | I/O pin source/sink current | | | -20 | | 20 | mA |
| $V_{IH}$ | High level input voltage | $V_{CC}$ = 2.7 - 3.6V | | 2 | | $V_{CC}$+0.3 | V |
| | | $V_{CC}$ = 2.0 - 2.7V | | 0.7*$V_{CC}$ | | $V_{CC}$+0.3 | |
| | | $V_{CC}$ = 1.6 - 2.0V | | 0.7*$V_{CC}$ | | $V_{CC}$+0.3 | |
| $V_{IL}$ | Low level input voltage | $V_{CC}$ = 2.7- 3.6V | | -0.3 | | 0.3*$V_{CC}$ | |
| | | $V_{CC}$ = 2.0 - 2.7V | | -0.3 | | 0.3*$V_{CC}$ | |
| | | $V_{CC}$ = 1.6 - 2.0V | | -0.3 | | 0.3*$V_{CC}$ | |
| $V_{OH}$ | High level output voltage | $V_{CC}$ = 3.0 - 3.6V | $I_{OH}$ = -2mA | 2.4 | 0.94*$V_{CC}$ | | |
| | | $V_{CC}$ = 2.3 - 2.7V | $I_{OH}$ = -1mA | 2.0 | 0.96*$V_{CC}$ | | |
| | | | $I_{OH}$ = -2mA | 1.7 | 0.92*$V_{CC}$ | | |
| | | $V_{CC}$ = 3.3V | $I_{OH}$ = -8mA | 2.6 | 2.9 | | |
| | | $V_{CC}$ = 3.0V | $I_{OH}$ = -6mA | 2.1 | 2.6 | | |
| | | $V_{CC}$ = 1.8V | $I_{OH}$ = -2mA | 1.4 | 1.6 | | |
| $V_{OL}$ | Low level output voltage | $V_{CC}$ = 3.0 - 3.6V | $I_{OL}$ = 2mA | | 0.05*$V_{CC}$ | 0.4 | |
| | | $V_{CC}$ = 2.3 - 2.7V | $I_{OL}$ = 1mA | | 0.03*$V_{CC}$ | 0.4 | |
| | | | $I_{OL}$ = 2mA | | 0.06*$V_{CC}$ | 0.7 | |
| | | $V_{CC}$ = 3.3V | $I_{OL}$ = 15mA | | 0.4 | 0.76 | |
| | | $V_{CC}$ = 3.0V | $I_{OL}$ = 10mA | | 0.3 | 0.64 | |
| | | $V_{CC}$ = 1.8V | $I_{OL}$ = 5mA | | 0.3 | 0.46 | |
| $I_{IN}$ | Input leakage current | | | | <0.001 | 0.1 | µA |
| $R_P$ | I/O pin Pull/Buss keeper resistor | | | | 25 | | kΩ |
| $R_{RST}$ | Reset pin pull-up resistor | | | | 25 | | |
| $t_r$ | Pad rise time | No load | | | 4.0 | | ns |
| | | | slew rate limitation | | 7.0 | | |

Figure 3: I/O Pin Specifications

# I/O Pin Characteristics - RDSout

- The Iol and Ioh specifications beg the question of actual DC output resistance.
- These values are easily found with a simple setup.
- The lower resistance of the N-channel transistor becomes evident when testing the I/O pin with a 50 ohm transmission. (later)

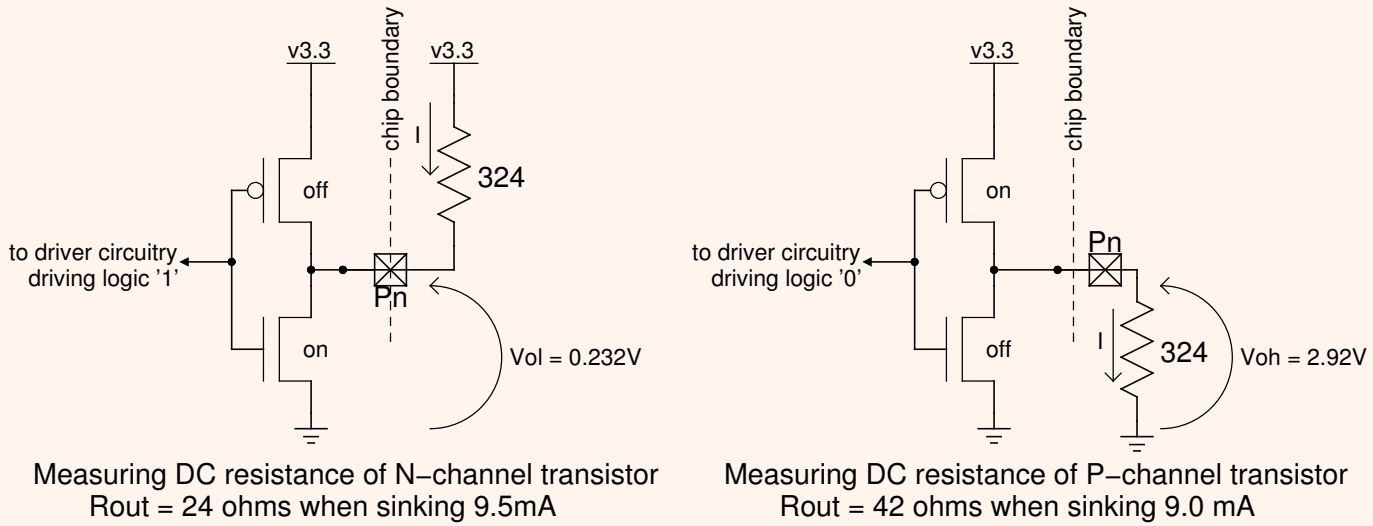



Figure 4: I/O Pin DC Equivalent Output Resistance

# I/O Pin Characteristics - PINnCTRL

- Each I/O pin has its own PINnCTRL register.
- PINnCTRL controls:
  - Output and Pull Configuration - 8 choices
  - Slew Rate Limit - fast or slow edges
  - Inverted I/O - inverted I/O or not
  - Input and Sense Configuration - mostly for interrupts

# I/O Pin Characteristics - Output and Pull

- The following schematics are not the actual circuitry of the xmega chip, but they are logically and electrically correct conceptual drawings of how each I/O configuration operates.
- In particular, a 24K resistor would be too costly from a area standpoint on silicon. The pullup and pulldown resistances are most likely implemented with weak (big L, small W) transistors.

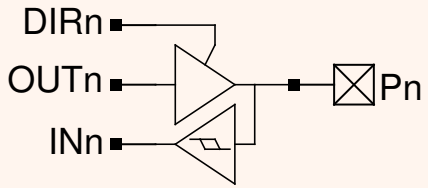
# I/O Pin Characteristics - Output and Pull

- Each I/O configuration was lab tested for their electrical and logical functionality. The assumption is that nothing is connected to Pn. Electrical characteristics for each configuration were tested as follows:
- Test for each Pn=Z case:
  - Connect 24K resistor from Pn to Vdd. Pn should be at Vdd.
  - Connect 24K resistor from Pn to Vss. Pn should be at Vss.
- Test for each Pn=0R case (logic '0' resistive):
  - Connect 24K resistor from Pn to Vdd. Pn should be at Vdd/2.
- Test for each Pn=1R case: (logic '1' resistive)
  - Connect 24K resistor from Pn to Vss. Pn should be at Vdd/2.

# I/O Pin Characteristics - Output and Pull

- Totem pole configuration able to source and sink current from Pn.
- Bi-directional, depending on the setting of the DIRn bit

```
\\set port B bit zero to totem pole
PORTB.PINOCTRL = PORT_OPC_TOTEM_gc;
```




| DIRn | OUTn | Pn | INn |
|---|---|---|---|
| 0 | 0 | Z | X |
| 0 | 1 | Z | X |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

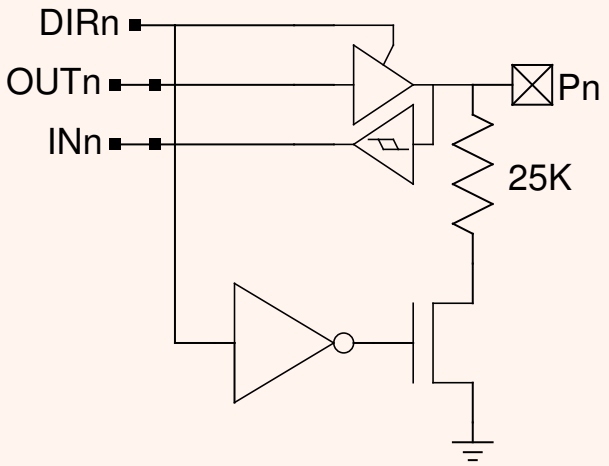
Truth Table

Figure 5: Totem Pole I/O

# I/O Pin Characteristics - Output and Pull

- Totem pole with pulldown is a totem pole configuration that depending on the DIRn bit, the input may be pulled down with a 25K resistance.
- Bi-directional, can sink or source current

```
\\set port B bit zero to totem pole with pulldown
PORTB.PINOCTRL = PORT_OPC_PULLDOWN_gc;
```




| DIRn | OUTn | Pn | INn |
|---|---|---|---|
| 0 | 0 | 0R | 0 |
| 0 | 1 | 0R | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

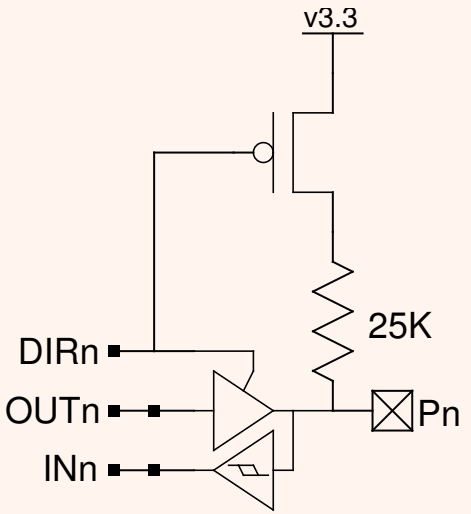
Truth Table

Figure 6: Totem Pole with Pulldown

# I/O Pin Characteristics - Output and Pull

- Totem pole with pullup is like the totem pole configuration but depending upon the DIRn bit, the input may be pulled up with a 25K resistance.
- Bi-directional, can sink or source current.

```
\\set port B bit zero to totem pole with pullup
PORTB.PINOCTRL = PORT_OPC_PULLUP_gc;
```




| DIRn | OUTn | Pn | INn |
|---|---|---|---|
| 0 | 0 | 1R | 1 |
| 0 | 1 | 1R | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

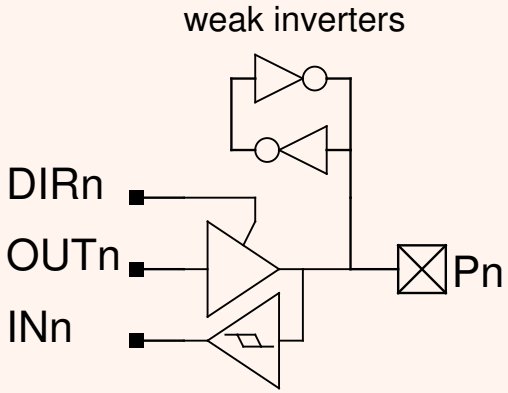
Truth Table

Figure 7: Totem Pole with Pullup

# I/O Pin Characteristics - Output and Pull

- Totem pole with bus keeper keeps the last value seen on PINn if driven from the output driver or external circuitry.
- The input will be pulled up or down with a 25K resistance
- Bi-directional, can sink or source current
- When selected, the bus keeper is active, regardless of the value of the DIRn bit

```
\\set port B bit zero to totem pole with bus keeper
PORTB.PINOCTRL = PORT_OPC_BUSKEEPER_gc;
```




| DIRn | OUTn | Pn | INn |
|---|---|---|---|
| 0 | 0 | $Pn^-$ | $Pn^-$ |
| 0 | 1 | $Pn^-$ | $Pn^-$ |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Bus Keeper Truth Table

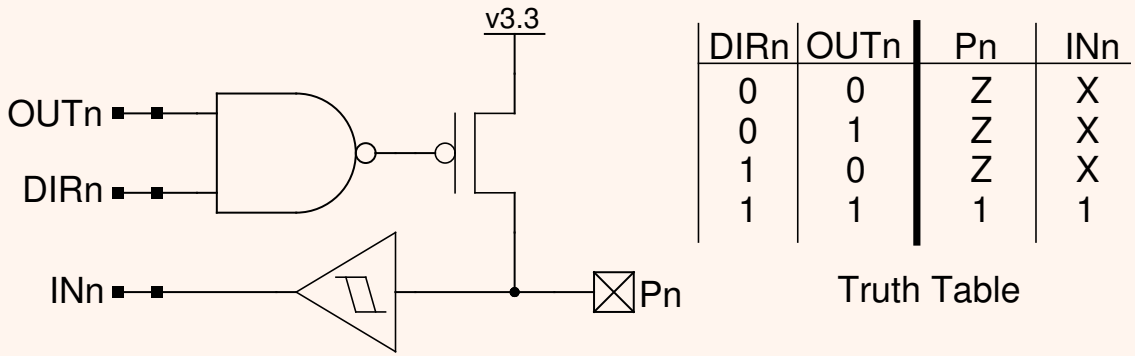
*$Pn^-$ : last value impressed on Pn

Figure 8: Bus Keeper

# I/O Pin Characteristics - Output and Pull

- Wired OR configuration is only able to source current
- When the DIRn bit is logic zero, the input buffer is floating.
- The wired OR is technically bi-directional, but can only source current.

```
\\set port B bit zero to wired OR
PORTB.PINOCTRL = PORT_OPC_WIREDOR_gc;
```




| DIRn | OUTn | Pn | INn |
|---|---|---|---|
| 0 | 0 | Z | X |
| 0 | 1 | Z | X |
| 1 | 0 | Z | X |
| 1 | 1 | 1 | 1 |

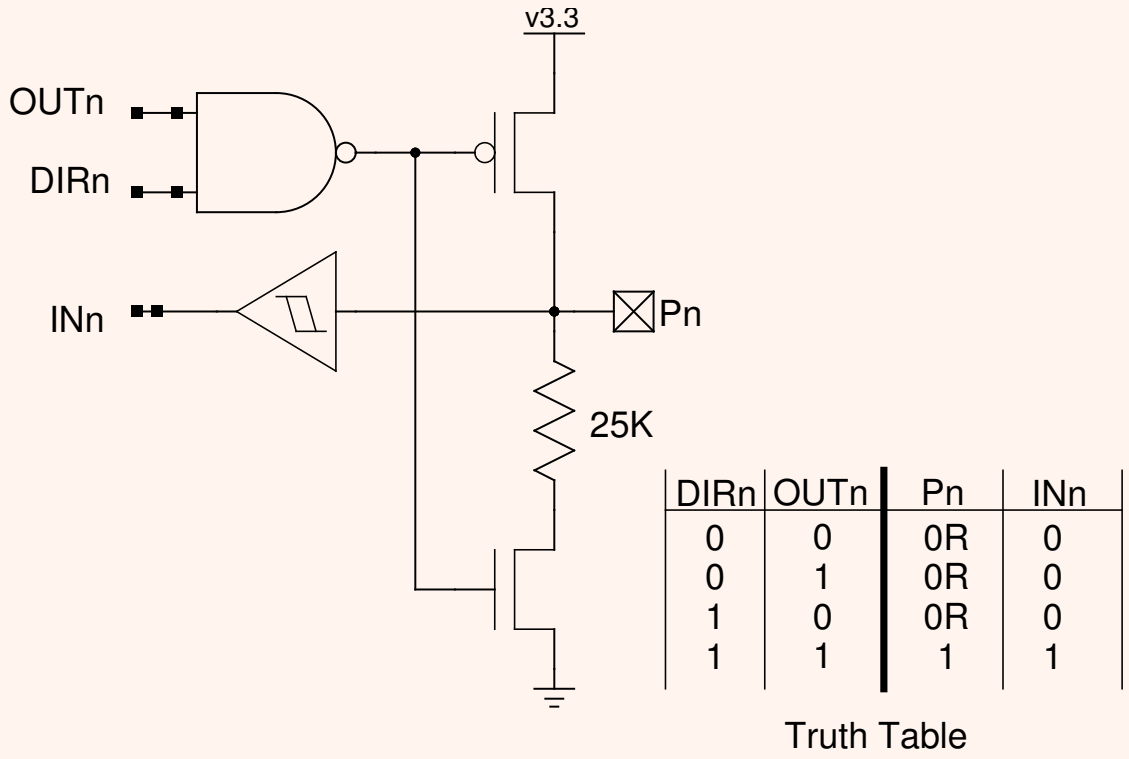
Truth Table

Figure 9: Wired OR

# I/O Pin Characteristics - Output and Pull

- Wired OR with Pulldown differs from Wired OR in that when the DIRn bit is logic zero, the input buffer is pulled down by a nominal 25K resistance

```
\\set port B bit zero to wired OR with a pulldown resistance
PORTB.PINOCTRL = PORT_OPC_WIREDORPULL_gc;
```



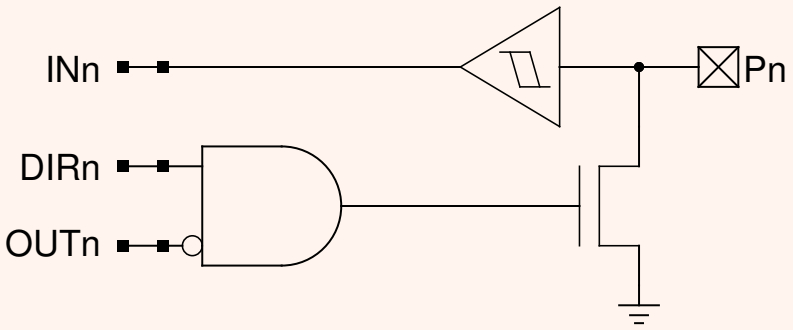

| DIRn | OUTn | Pn | INn |
|---|---|---|---|
| 0 | 0 | 0R | 0 |
| 0 | 1 | 0R | 0 |
| 1 | 0 | 0R | 0 |
| 1 | 1 | 1 | 1 |

Truth Table

Figure 10: Wired OR with Pulldown

# I/O Pin Characteristics - Output and Pull

- Wired AND configuration is bi-directional and only able to sink current



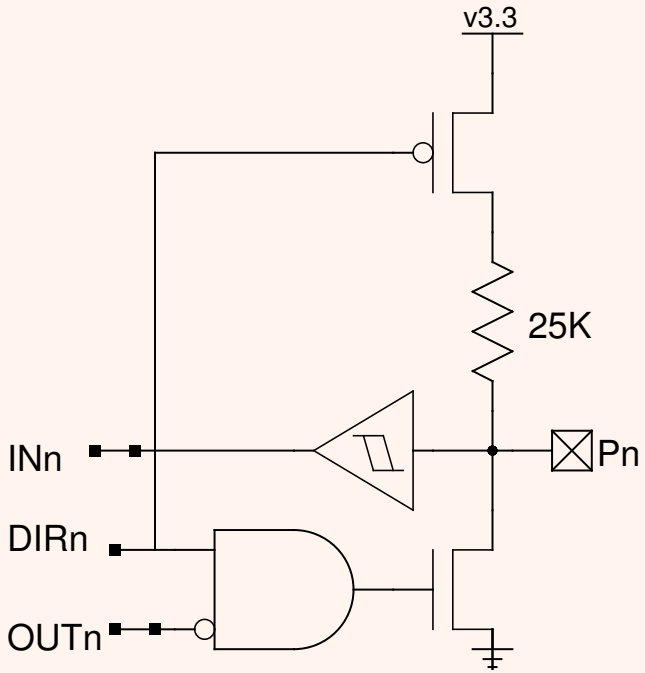

| DIRn | OUTn | Pn | INn |
|---|---|---|---|
| 0 | 0 | Z | X |
| 0 | 1 | Z | X |
| 1 | 0 | 0 | 0 |
| 1 | 1 | Z | X |

Truth Table

Figure 11: Wired AND

# I/O Pin Characteristics - Output and Pull

- Wired AND configuration is bi-directional and only able to sink current




| DIRn | OUTn | Pn | INn |
|---|---|---|---|
| 0 | 0 | 1R | 1 |
| 0 | 1 | 1R | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 1R | 1 |

Truth Table

Figure 12: Wired And with Pullup

# I/O Pin Characteristics - Output and Pull

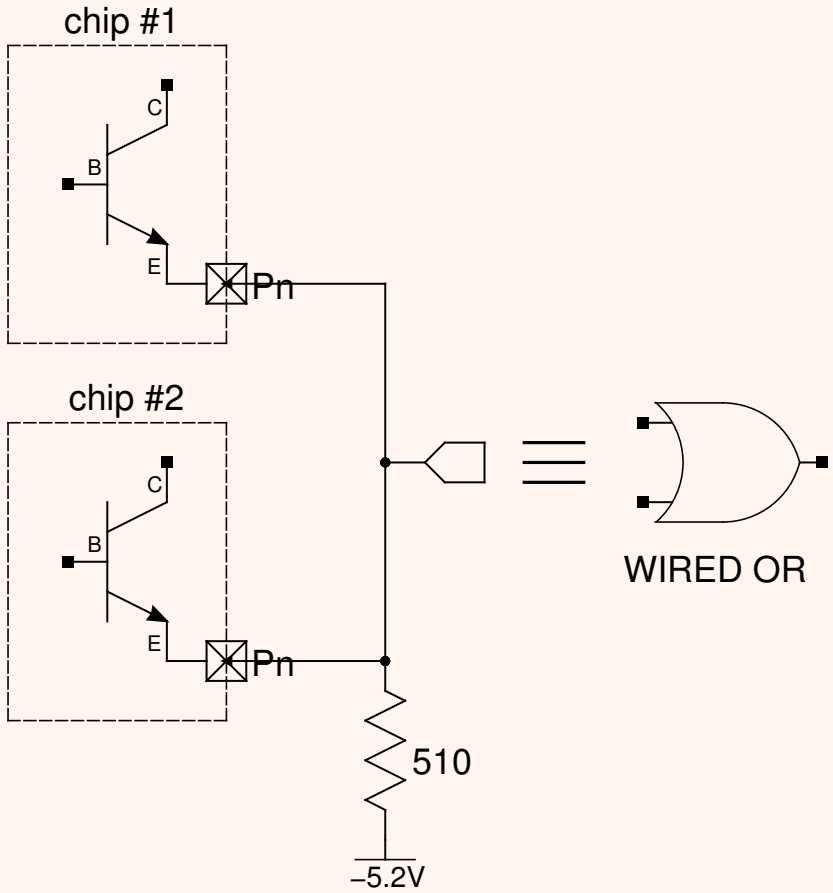



Figure 13: Wired OR as used in Emitter Coupled Logic

# I/O Pin Characteristics - Output and Pull

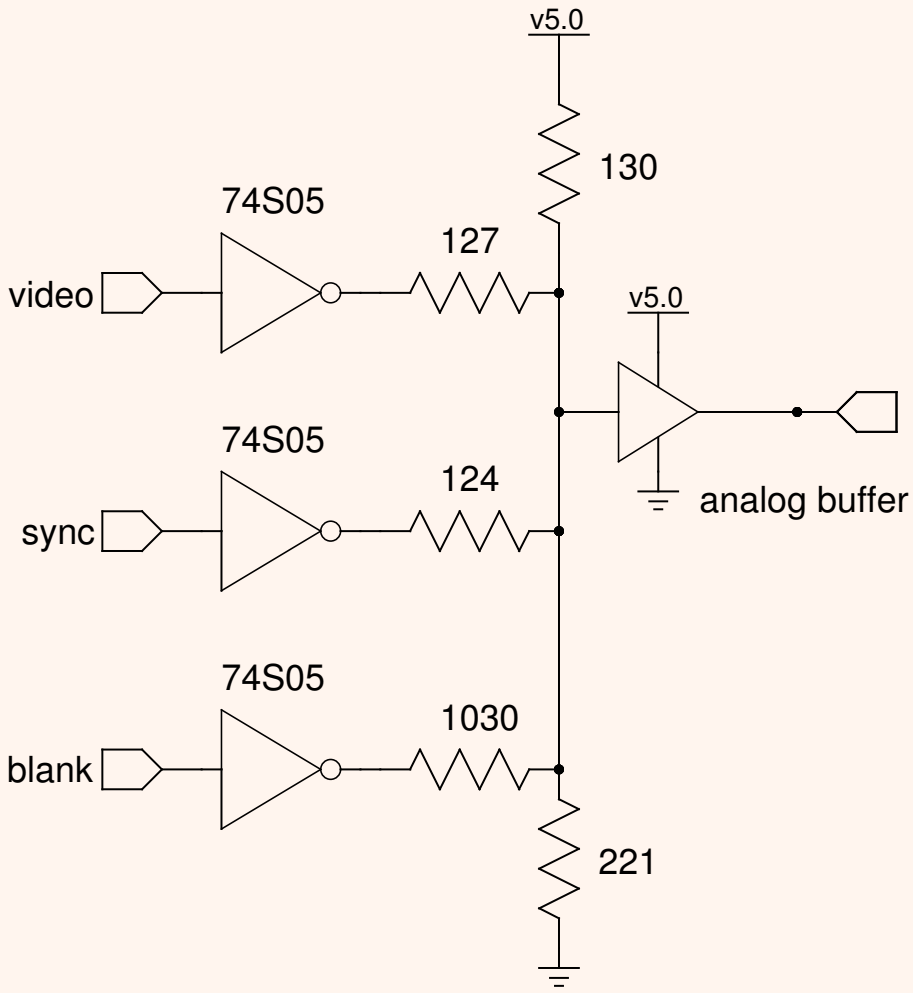



Figure 14: Wired AND VGA Level Generator in STTL Logic

# I/O Pin Characteristics - Output and Pull

- I2C interface uses wired AND configuration
- Any I/O can pull the SCL or DAT line down without conflict.
- Any I/O can be a driver or receiver
- External pullups must be used for pull the lines up.
- Pullups must be sized to pull up capacitance on the signaling lines

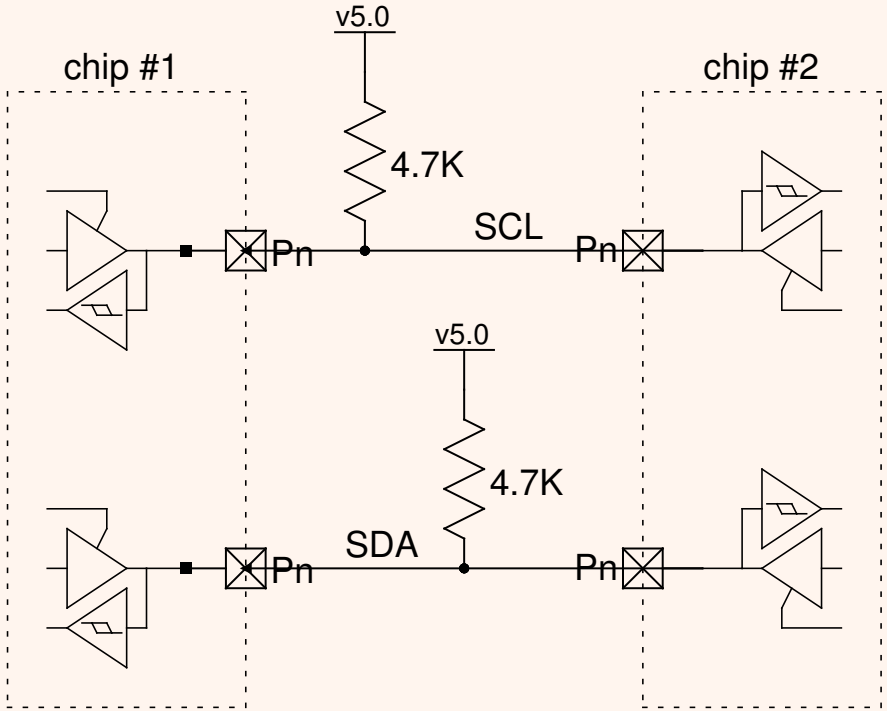



Figure 15: I2C Interface using Wired AND Configuration

# I/O Pin Characteristics - Slew Rate

- Each I/O pin has a SRLEN bit within its PINnCTRL.
- SRLEN controls how much current the pin can supply on an edge.
- It does not effect the DC current capability of the pin.
- When set, the pin is limited to a 7ns rise and fall time.
- When clear, the pin operates with a 4ns rise and fall time.
- Spec is written for no load.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $t_r$ | Pad rise time | No load | | | 4.0 | | ns |
| | | | slew rate limitation | | 7.0 | | |

Figure 16: Slew Rate Control Specification

# I/O Pin Characteristics - Slew Rate

- Lab measurements

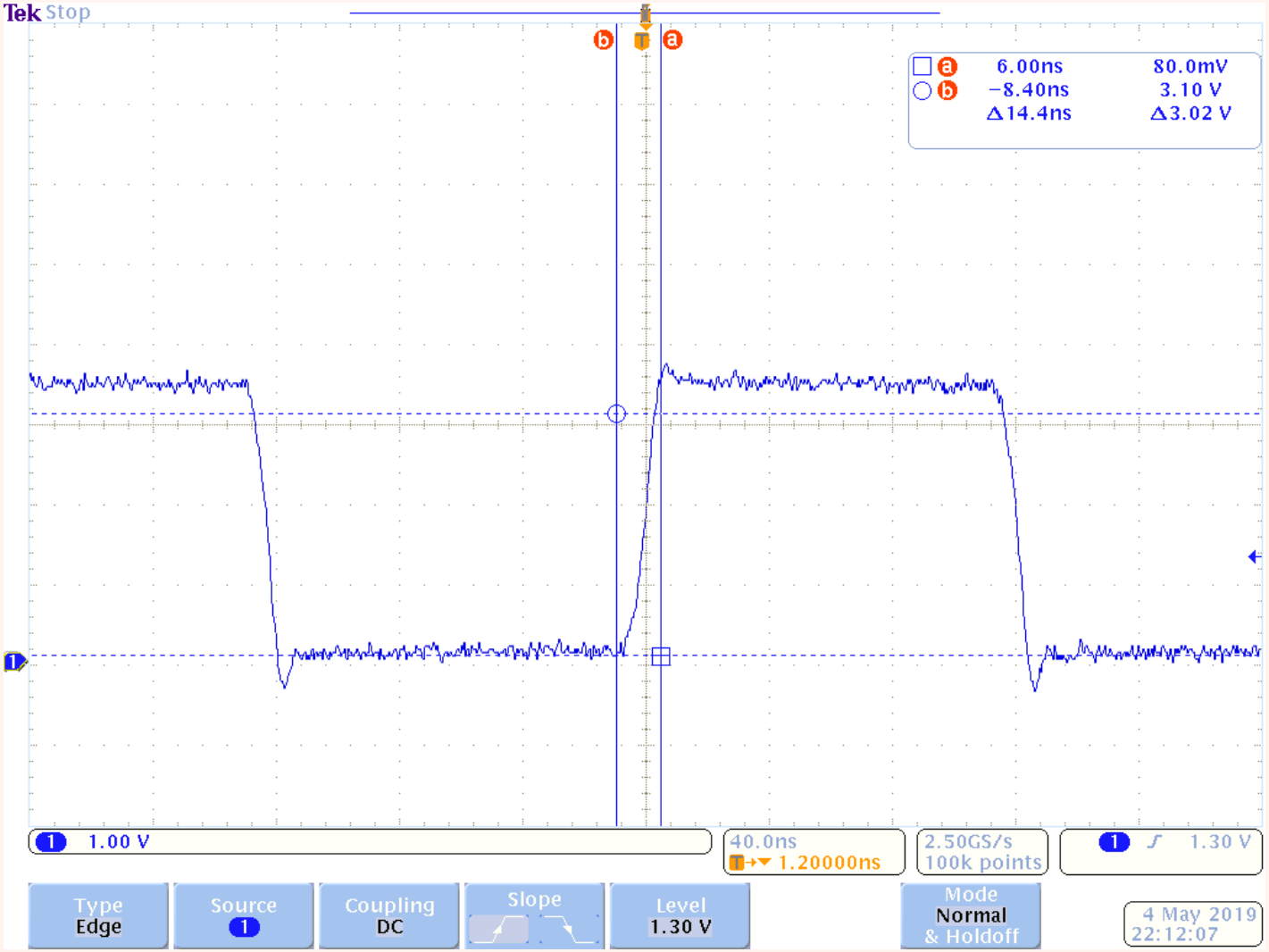



Figure 17: Slew Rate Control On

# I/O Pin Characteristics - Slew Rate

- Lab measurements

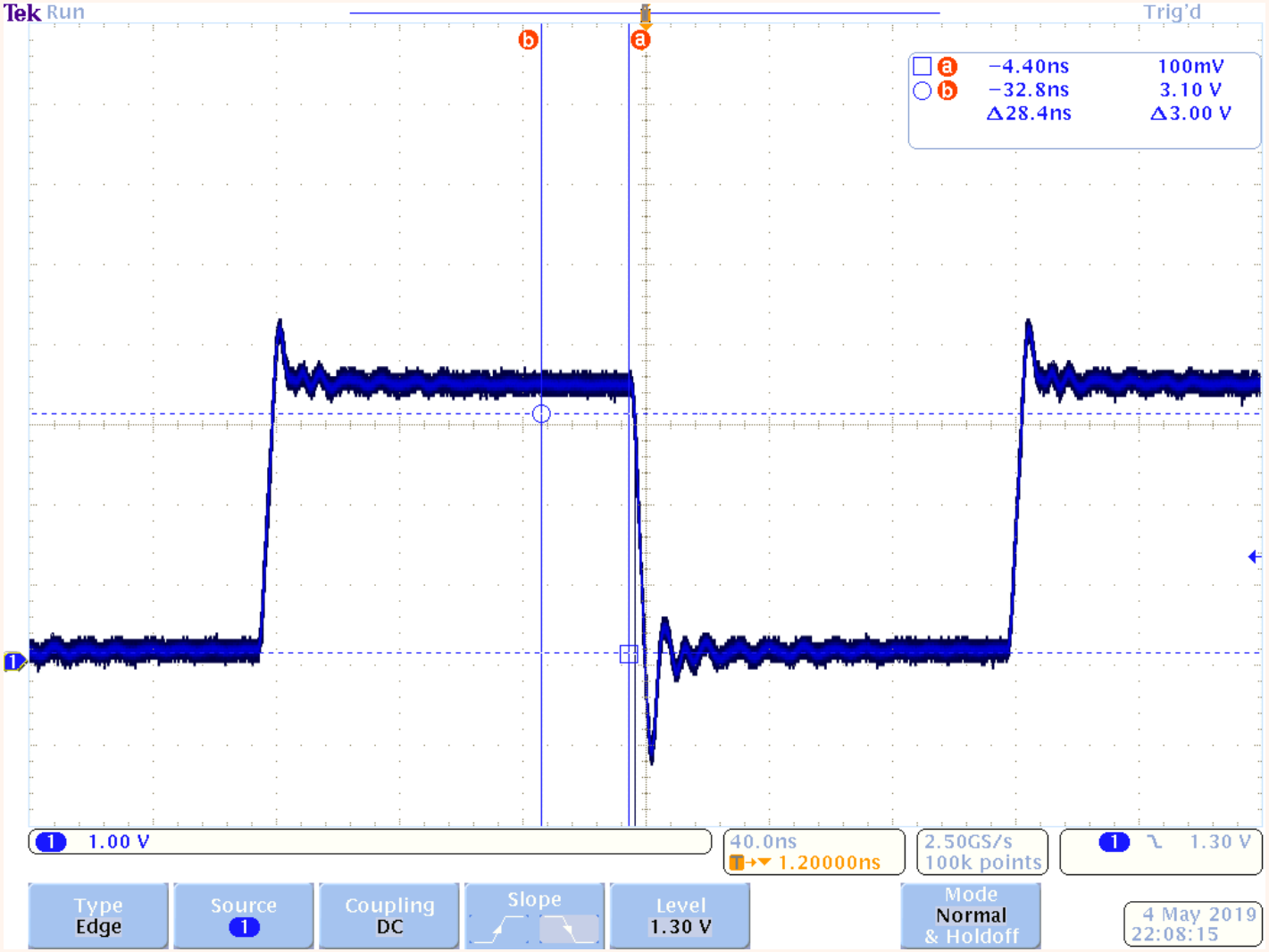



Figure 18: Slew Rate Control Off

# I/O Pin Characteristics - Slew Rate

- Lab measurements clearly indicate that the I/O pins are incapable of incident-wave switching
- A point-to-point connection on a 50 ohm line is however possible.
- Scope probe is at the I/O pin


Figure 19: I/O pin driving 50 ohm transmission line

# I/O Pin Characteristics - Output impedance

- Lab measurements would indicate the dynamic output resistance is approximately 50 ohms