ECE 474 - Quiz 1 - Spring 2017

Name and last 4 digits of ID: _____

1. [10] When vlog is invoked on an rtl-level file such as fadder.sv, what input file is necessary?

   Just the rtl file is necessary.

2. [10] What does vlog do when invoked up on a file such as fadder.sv?

   It produces an executable file for the simulator

3. [10] What two input files must exist in /work before vsim can be invoked on a gate-level design. (description of the files, not their actual names)

   The compiled or executables for the design and the gates

4. [10] What does the simulation "do file" do?

   It tells it how to run, forcing of signals, which ones to display, etc.

5. [10] How did the contents of sv and gate.v differ?

   *.sv is an rtl-level design behavioral description, the *.gate.v is a netlist of gates that represents the design.

6. [10] What was the biggest difference between rtl and gate simulation results?

   The gate simulation shows gate delays.

7. [15]What is "*design_analyzer*" used for?

   It produces a gate level realization of our design as well as implementation information such as size and speed.

8. [10] What two input files are provided to *design_analyzer*?

   - The input rtl file and .synopsys_dc_setup
   - (cell library is an alternative answer for the .synopsys_dc_setup file)

9. [15] What library does the *.synopsys_dc_setup* file point to?

   - The cell library