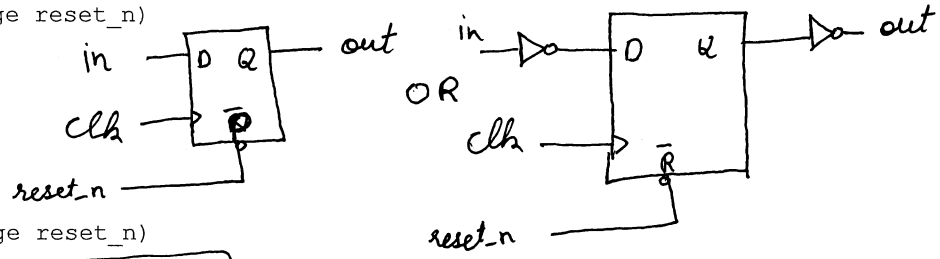
ECE474/574 Quiz 2 5.8.2017

Name:_____

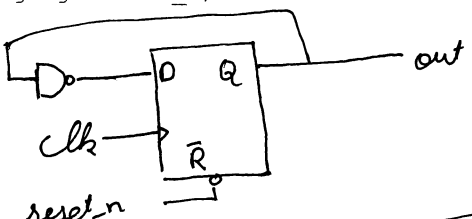
Draw the logic created by the following code. Use only D-type FFs/latches, muxes, and combinatorial logic. Label all pins and wires. Assume the input and output signals have been previously defined.

```
always_ff @ (posedge clk, negedge reset_n)
  if(!reset_n)
    out <= '1;
  else
    out <= in;
```



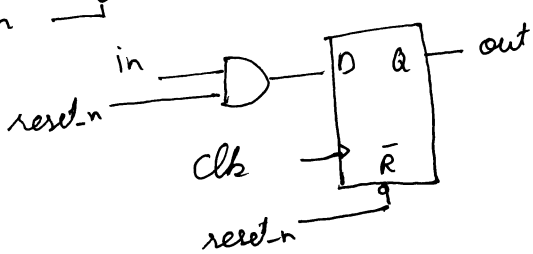
reset applied to preset pin

```
always_ff @ (posedge clk, negedge reset_n)
    if(!reset_n)
      out <= '0;
    else
      out <= ~out;
```



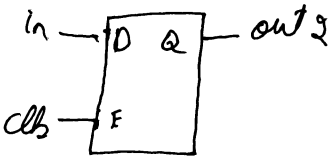
reset applied to reset pin

```
always_ff @ (posedge clk)
      if (!reset_n)
        out <= '0;
      else
        out <= in;
```



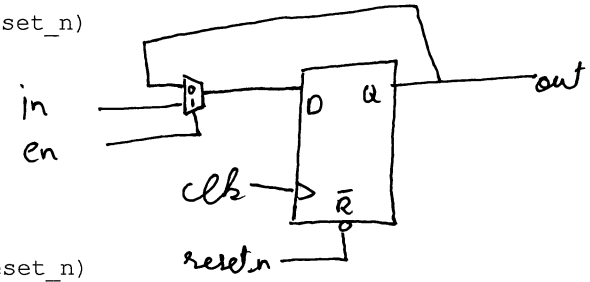
syn reset

```
always_latch
    if (clk) out2 <= in;
```



Positive latch enable

```
always_ff @ (posedge clk, negedge reset_n)
    if(!reset_n)
      out <= '0;
    else
      if (en == 1'b1)
        out <= in;
```




```
always_ff @ (posedge clk, negedge reset_n)
    if(!reset_n) begin out  <= '0; out1 <= '0;  end
    else         begin out  <= in; out1 <= out; end
```