ASICs - What are they?

- An ASIC is:
  - An Application Specific Integrated Circuit
  - An ASIC is an IC that is designed to perform a particular, specialized function
  - It is not software programmable, unless its a uC
  - It is not not a memory chip, but may contain memory
- Examples would include
  - MPEG decoder
  - Audio processor for Dolby noise reduction
  - Image processor for MRI
- How are ASICs used?
  - Many popular electronic devices
  - High volume, cost sensitive
  - High reliability, high performance (mA/Mhz)

ASICs - Types of ASICs

- Full Custom ASIC
  - Each transistor hand drawn, (polygon pushing)
  - Analog parts are done this way
  - Highest performance, longest design time
  - Hand optimized parts of high-end uPs
  - Full set of masks needed

ASICs - Types of ASICs

- Standard Cell ASIC
  - Predesigned (standard) cells in a library are used
  - These cells are connected together to form the design
  - High performance, much shorter design time than full custom
  - Most digital ASICs are designed this way
  - Usually uses HDLs with logic synthesis
  - Full set of masks needed

ASICs - Types of ASICs

- Gate Array ASIC
  - Predrawn transistors are on a die
  - These transistors are connected together to form cells
  - The cells are connected to form a design
  - Usually digital in nature
  - Lower performance, but very quick to fabricate
  - Only metalization masks are needed
  - Usually uses HDLs with logic synthesis

ASICs - Types of ASICs

- FPGA
  - Fully predesigned silicon, logic functions and interconnect
  - Programmed with a "bit file" to configure logic and interconnect
  - Medium performance, higher power consumption
  - Very quick to implement, minutes
  - Better for more limited volume applications
  - Almost always uses HDLs plus logic synthesis
  - No DFT structures required
  - Popular for ASIC prototyping

ASICs - Considerations?

- Time to market
  - Time to market is a primary driver
  - Dramatic increase in profit with earlier time-to-market landing
  - Cutting one month off schedule increases profit roughly 10%

ASICs - Considerations?

- Cost
  - Standard cell synthesis can cost $125k per license
  - Typical standard cell NRE $50K to $200K
  - If you can't spend at least a million, you are not in the game
  - One bug in a standard cell design can be a disaster
  - A standard cell "respin" takes possibly 8 weeks and a lot of money
  - Really cheap tools are available for FPGA implementation - free!
  - FPGAs cost $10-100 each in single quantity
  - FPGA bugs are fixed at zero cost in minutes

Mask set costs (2006)

Process(um)	Vdd	Metal layers	Mask Set Cost ($)
65	1.0	9	3,000,000
90	1.0	9	1,500,000
130	1.2	7	750,000
350	3.3	3	40,000

ASICs - How do you choose?

- 1 - Technical feasibility
  - Can it run fast enough?
  - Is it low enough power?
  - Can it operate at 1.2V?
  - Is the required IP available?
- 2 - Financial Analysis
  - What is the cost to get first prototypes (NRE)
  - What is the volume piece part price?
  - How many will we ship?
  - How much market share would we loose?
- Roughly: FPGAs for volumes $<$1000's, ASICs for volumes $>$10,000