```
case (case_expression)
  case_item1 : case_item_statement;
  case_item2 : case_item_statement;
  case_item3 : case_item_statement;
      :
  default    :
endcase
```

Verilog has implied "break" stmt unlike "C"
case items are non-overlapping in VHDL, but not Verilog.

---

unique case

- unique is an assertion
  - → All possible values for case_expression are in list of case_items
  - → At run time, a match must be found in case_items
  - → At run time, only one match will be found in case_items
- unique guides synthesis
  - → it indicates that no priority logic is necessary, parallel logic may be produced (faster, smaller)
- unique usage
  - → use when each case_item is unique and only one match should occur
  - → using "default" removes testing for non-existant matches, but uniqueness test remains.

# priority case

- priority is an assertion
  - → All possible values for case_expression are in the list of case_items
- priority guides synthesis
  - → it indicates that all other testable conditions are don't cares and may be used to simplify logic.
- priority usage
  - → use to explicitly say that priority is important
  - → including "default" will cause priority requirement to be dropped since all cases are available to be matched
  - → it also indicates that more than one match in case_items is OK.
- priority is a bad name
  - → case is always a priority structure