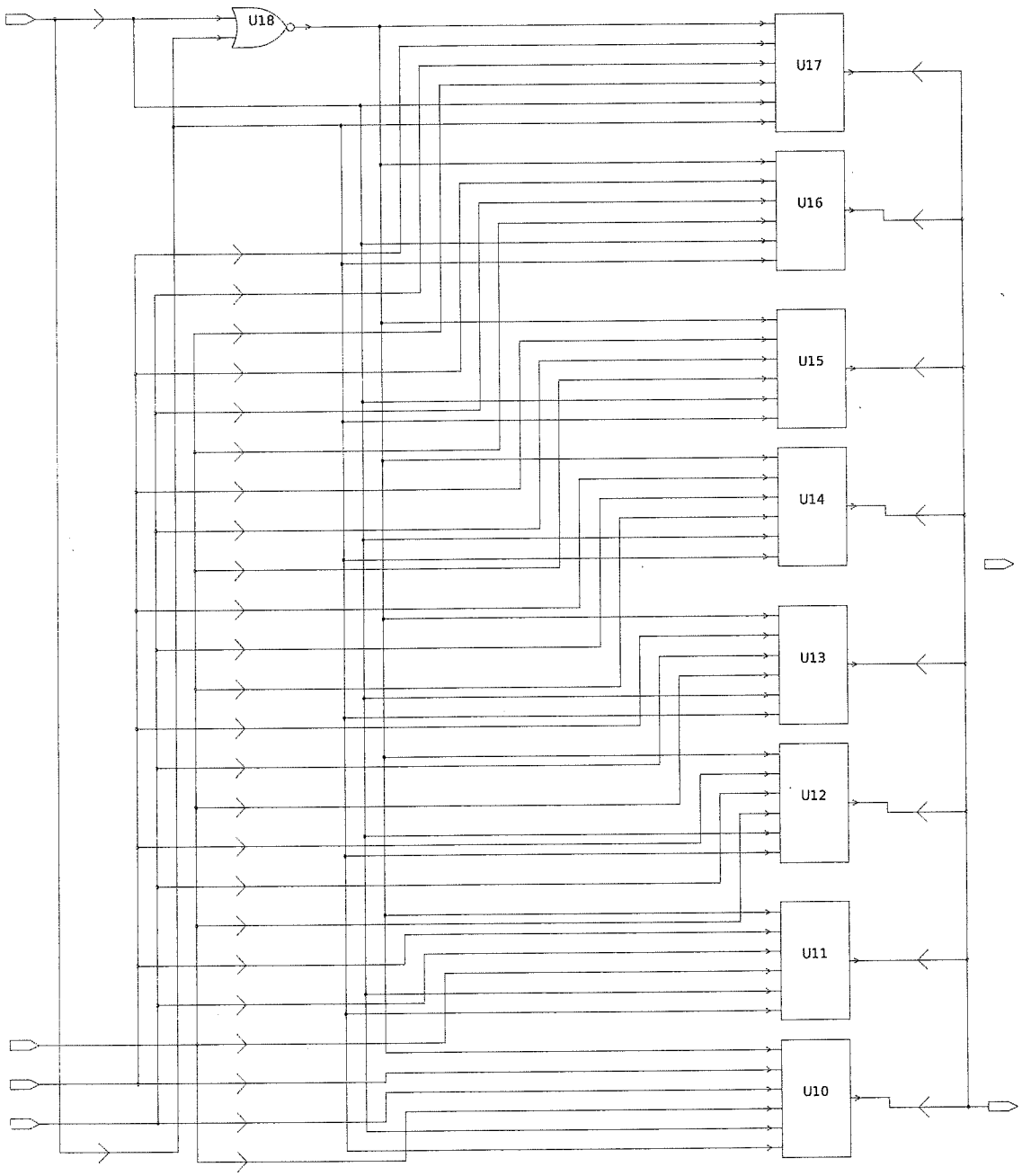
UNIQUE CASE

```
module case2(
input       [7:0] a_in, b_in, c_in, d_in,
input       [1:0] sel,
output reg  [7:0] d_out);

always_comb
  unique case (sel)
    2'b00    :  d_out = a_in;
    2'b01    :  d_out = b_in;
    2'b10    :  d_out = c_in;
  endcase
endmodule
```

AREA = 129.3

DELAY = 12.31



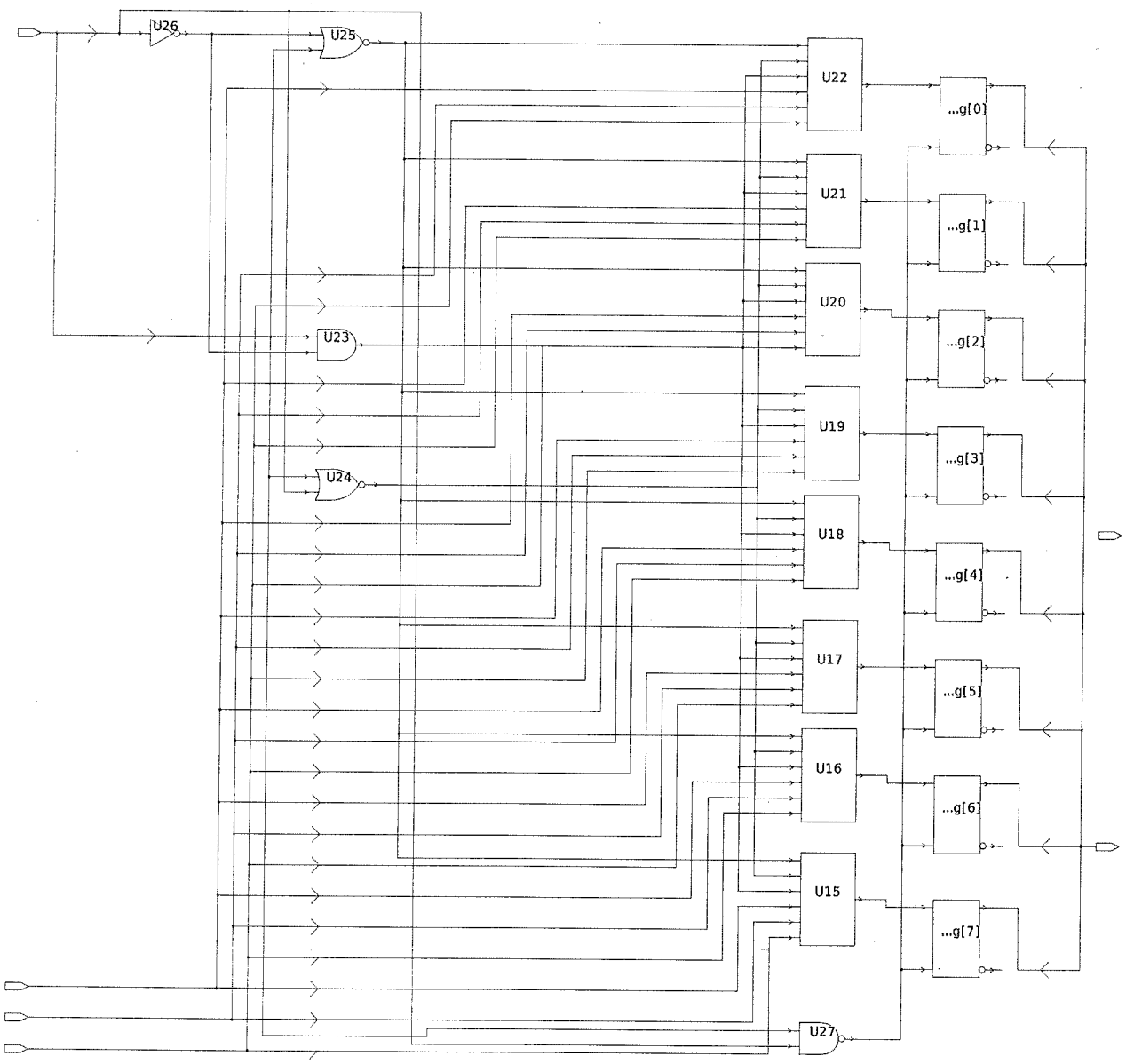
CASE W/O UNIQUE

```
module case2(
input       [7:0] a_in, b_in, c_in, d_in,
input       [1:0] sel,
output reg  [7:0] d_out);

always_comb
  case (sel)
    2'b00    :  d_out = a_in;
    2'b01    :  d_out = b_in;
    2'b10    :  d_out = c_in;
  endcase
endmodule
```

AREA = 339.1

DELAY = 12.45

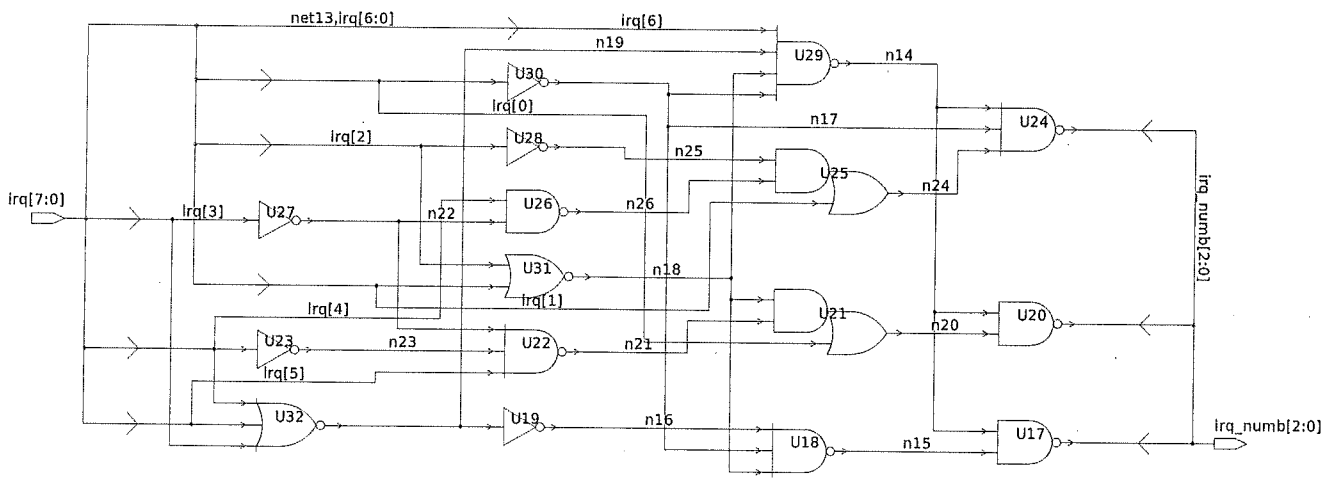


CASEZ W/O PRIORITY

```
module int_dec4(
  output  reg  [2:0] irq_numb,
  input        [7:0] irq
);

always_comb
  begin
    irq_numb=4'b0000;  //case where there is no interrupt
    casez (irq)
      8'b???????1: irq_numb=4'b0001; //interupt zero, ignore other bits
      8'b??????10: irq_numb=4'b0010; //interupt one , ignore other bits
      8'b?????100: irq_numb=4'b0011;
      8'b????1000: irq_numb=4'b0100;
      8'b???10000: irq_numb=4'b0101;
      8'b??100000: irq_numb=4'b0110;
      8'b?1000000: irq_numb=4'b0111;
      8'b10000000: irq_numb=4'b1000;
    endcase
  end
endmodule
```

AREA 111.95
DELAY 9.97



CASEZ WITH PRIORITY

```
module int_dec4(
  output  reg  [2:0] irq_numb,
  input        [7:0] irq
);

always_comb
  begin
    irq_numb=4'b0000;  //case where there is no interrupt
    priority casez (irq)
      8'b???????1: irq_numb=4'b0001; //interupt zero, ignore other bits
      8'b??????10: irq_numb=4'b0010; //interupt one , ignore other bits
      8'b?????100: irq_numb=4'b0011;
      8'b????1000: irq_numb=4'b0100;
      8'b???10000: irq_numb=4'b0101;
      8'b??100000: irq_numb=4'b0110;
      8'b?1000000: irq_numb=4'b0111;
      8'b10000000: irq_numb=4'b1000;
    endcase
  end
endmodule
```

AREA 111.91

DELAY 4.32 nS