Verilog - Signal Objects

- There are two types of signal object, *net* and *variable*

**Nets**
- Model connections (wires and busses) in structural descriptions
- Defaults to 4-state data type
- Has conflict resolution with multiple drivers
- `wire [7:0] mybus;`
- Use *wire* to connect modules
- Use *logic* to create logic

**Variables**
- Stores values assigned in initial, always, task and function blocks
- Used to describe logic behavioral modeling
- `logic [4:0] nibble_en;`