Intro to Verilog

Verilog History

- Developed by Gateway Design Automation (1984)
- Proprietary hardware simulation and verification tool only
- Influenced by HiLo (old HDL language) and C
- Fault simulation, timing analyzer and synthesis ready 1987
- Cadence Design Systems bought Gateway (and Verilog) in 1990
- Cadence marketed it as a language and simulator, Verilog-XL

Intro to Verilog

Verilog History(cont.)

- VHDL influence
  - VHDL driven by DOD VHSIC program
  - Based on Ada
  - Vhsic Hardware Design Language = VHDL
- Cadence recognized a closed language was doomed
- Standardization would win the day eventually
- Cadence organized Open Verilog International (OVI) and gave language away
- Others were trying to alter the language for their benefit
- IEEE 1364 working group made Verilog IEEE std. 1364-1995
- Verilog 95 finished in 1995 (duh!)

Intro to Verilog

Verilog History(cont.)

- Other Verilog simulators than Cadence Verilog-XL available (1992)
- Verilog Compiled Simulator (VCS) from Chronologic: very successful
- VCS eventually bought by Synopsys
- Modelsim (Mentor), a very good mixed language simulator
- The big three simulators (all sign-off quality) are:
  - Modelsim [Mentor]
  - NC-Verilog [Cadence] (derived from Verilog-XL)
  - VCS [Synopsys] (derived from Chronologic VCS)
- Icarus Verilog [open source] (not fully 1356-2001 compliant)

Intro to Verilog

Verilog History(cont.)

- Verilog 2001 fixed many shortcomings Verilog 95 had
- System Verilog is a super-set of Verilog 2001
- System Verilog born from the need to unify design and verification
- Adds VHDL features and design verification improvements
- Both Verilog and VHDL have analog extensions VHDL-A and Verilog-AMS

Intro to Verilog

Verilog and VHDL Compared

Verilog	**VHDL**
Weakly typed	Strongly typed
Looks like C	Looks like Ada (Pascal)
Case sensitive	Case insensitive
Terse	Verbose
Design by a few	Design by committee
Used all over	Mandated by government
Easy to learn	Harder to learn
Easy to screw up	Holds your hand closely