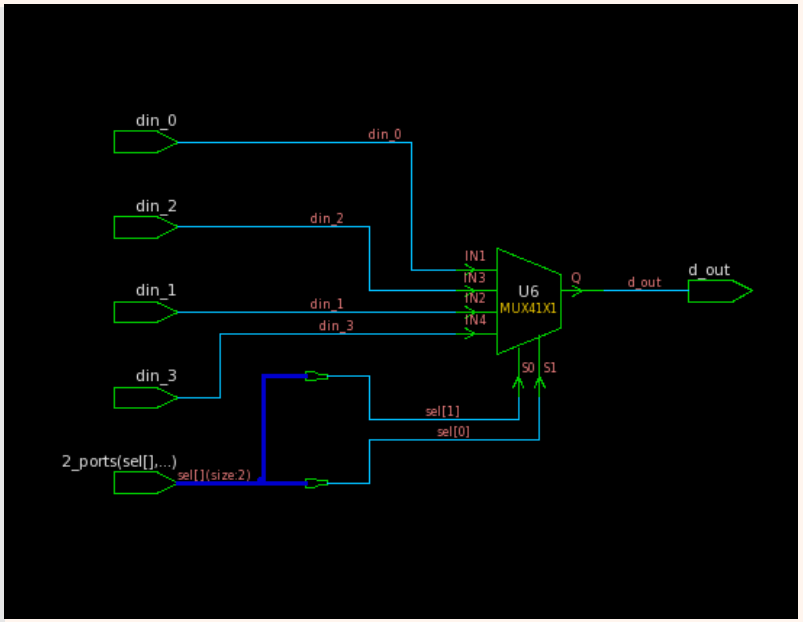
System Verilog - Part 4

- `if` becomes confusing beyond about 3 levels.
- `case` also creates combinatorial logic.
- When the case selection item matches the case expression, the corresponding assignments are made.

```
module mux4_1 (
  input  sel,
  input  din_0, din_1, din_2, din_3;
  output logic d_out);
  always_comb
    case(sel)
      2'b00  :  d_out = din_0;
      2'b01  :  d_out = din_1;
      2'b10  :  d_out = din_2;
      2'b11  :  d_out = din_3;
    endcase
endmodule
```



System Verilog - Part 4

- If multiple statements are selected by a case selection item, they must be bracketed by `begin` and `end`.

```
always_comb
  unique case (done_sm_ps)
   NOT_DONE:
     begin
       done = 1'b0;  //not done indication
       if((cycle_cnt==5'd31) & (mult_sm_ps==SHIFT))
         done_sm_ns <= DONE;
       else
         done_sm_ns <= NOT_DONE;
     end
   DONE:
     begin
       done = 1'b1;  //indicate done
       done_sm_ns <= NOT_DONE;
     end
  endcase
```