# Verilog - Signal Objects

- There are two types of signal object, *net* and *variable*

## Nets

- Model connections (wires and busses) in structural descriptions
- Defaults to 4-state data type
- Has conflict resolution with multiple drivers
- `wire [7:0] mybus;`
- Use `wire` to connect modules
- Use `logic` to create logic

## Variables

- Stores values assigned in initial, always, task and function blocks
- Used to describe logic behavorial modeling
- `logic [4:0] nibble_en;`

# signal objects

## net

models connections (wires, busses) in structural descriptions. Can also be target of cont. assignment

net types:
- wire
- uwire (unresolved wire, only one driver)
- wAnd
- wor
- tri
- triAnd
- trior
- tri0
- tri1
- triReg
- supply0 — supply strength (Vss)
- supply1 — supply strength (Vdd)

defaults to 4-state logic data type
wire can be explicitly defined as 4-state
- wire logic [2:0] data

conflict resolution for wire or tri

| | 0 | 1 | X | Z |
|---|---|---|---|---|
| 0 | 0 | X | X | 0 |
| 1 | X | 1 | X | 1 |
| X | X | X | X | X |
| Z | 0 | 1 | X | Z |

## variable

variables store values assigned in initial, always, task and function blocks. Used in behavioral modeling.

data type:

4-state (0, 1, X, Z)
- logic — user defines size, unsigned, init to 'X'
- reg — user defined size, unsigned, init to 'X'
- integer — 32-bit, signed, init to 'X'
- time — 64-bit, unsigned, init to 'X'

2-state (0, 1)
- bit — user defined size, unsigned, init to 0
- byte — 8-bit, signed, init to 0
- shortint — 16-bit, signed, init to 0
- int — 32-bit, signed, init to 0
- longint — 64-bit, signed, init to 0

= synthesizible

implicity variables
"logic" and "bit" are unsigned, remainder are signed
"logic" used by itself implies its a variable (var logic [2:0] data)
"var" by itself implies "logic"

Use logic to describe logic
Use int for loop variables
declare all nets at top of module

`default_nettype none
outlaw implicit declarations