ECE474/574 - Lab 2

Introduction

This lab will help you get familiar with reading inputs, assigning outputs, and the basics of SystemVerilog. You will also need to do some hardware building to complete this project. For this lab you will need to make a 8 to 3 encoder.

Assignment

First, you will need to assemble your push button board. Figure 1 shows the push button schematic. For this class we will not be using the 74LVC1G125 buffer supplied on the board. Instead you will tie `SW_COM` to ground and connect J1-J8 to pins on the DE0-Nano board with weak pull up resistors enabled. This will allow you to read when a button is pressed, causing that pin to go to ground.

Use the skeleton code provided to make your project. Your project will read in the 8 push buttons and map each button to the binary equivalent of that button. For example, if you push button 5 (of button 1 - button 8) then the LEDS will display a binary 5, and pushing button 8 will display a binary 8.

In addition, you will implement two different ways to encode the buttons to their binary equivalent. You will select between the two different methods using the slide switch on the board.

In order to turn on weak pull up resistors you must first run Analysis and Synthesis. After this open up your .qsf file in the project directory and add the following:

```
set_instance_assignment -name WEAK_PULL_UP_RESISTOR ON -to buttons
```

Alternatively, you can go to Assignments ⇒ Assignment Editor and scroll to the bottom of the Assignment Editor window. In the `<<new>>` row, in the `To` column type `buttons`, in the `Assignment Name` column select `Weak Pull-Up Resistor` and make sure `Value` is set to `On`.

You can click here for more information on the 8 push button board from Tekbots

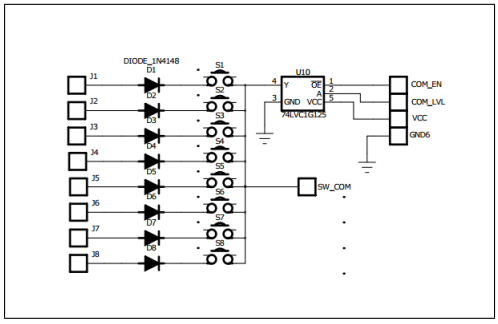

Figure 1: Push Button Schematic

Simulating

As the assignments get more complex it will be to your benefit to simulate before programing your FPGA. This will help you determine what is wrong with your code and fix it. Refer to lab1 for more information on how to simulate the design.

Checkoff

This week you will need to upload your code and a block diagram to TEACH along with getting it checked off in person. Program the FPGA in front of a TA and demonstrate the working code.