

ECE474/574 - Lab 5

Introduction

In this lab, we will construct a Direct Digital Synthesis (DDS) engine. Using a look-up table stored in a on-chip ROM, we will output a sine wave by using a R2R resistor network as a digital-to-analog converter (DAC). Instead of having a fixed output frequency or one that is tied directly to the input clock, the DDS allows us to output a variable frequency by having essentially two counters. One counter indexes the ROM, the other counter tells the indexing ROM when to advance.

Assignment

Since we are only outputting a sine wave, the memory will not need to change. Because of this, we will use the Cyclone IV's on-chip ROM (Read-Only Memory). It will be initialized at configuration time to hold the integer coefficients for a sine wave. This will be done by using a Altera .mif file (given to you with the lab) containing all of the sine wave values. The DDS phase accumulator will step through the ROM addresses, outputting the digital bits to the R2R network. Continuously looping through the ROM you output a sine wave.

You will use the encoders to change the frequency of the sine wave in increments of 1Hz going from 0Hz to 9999Hz. Display the frequency in Hz on the four-digit seven segment display. At power-up, your DDS unit should output a 1Khz signal and display "1000" on the display. Leading zero suppression is expected. No dimming is required. You will be supplied a 8-bit R2R network.

Checkoff

You will need to upload your code and a block diagram to TEACH along with getting it checked off in person. Program the FPGA in front of a TA and demonstrate the working code. The total utilization of logic elements will be bounded. In other words, efficient verilog code is expected. A minimum and maximum size in logic elements (LE's) will be specified shortly.