Cyclone IV Architecture - Logic Element (LE)

- Smallest units of logic in the IC
- Four-input LUT (LE)
- Programmable Register
- Carry Chain and Register Chain Connection

The image shows a block diagram of a Logic Element (LE) in a Cyclone IV device. The LE consists of a Look-Up Table (LUT), a Carry Chain, and a Programmable Register. The LUT is connected to various inputs and outputs, including data lines, clock enable, clear, and register feedback signals. The diagram illustrates how these components interact to perform logical operations and control signals.
Normal Mode
Retains 4-input LUT
For General Logic Applications
Cyclone IV Architecture - Logic Element (LE)

- **Arithmetic Mode**
- **Two 3-input LUTs**
- **For Adders, Counters, Accumulators, Comparators**
- **LE implements two-bit full adder, and carry chain**
Cyclone IV Architecture - Logic Array Blocks

- Logic Array Blocks contain 16 LEs
- Hierarchical routing resources, inter-LAB, extra-LAB
- Allows choosing of optimum wiring resource

![Diagram of Logic Array Blocks]

- 16 LEs
- LAB control signals
- LE carry chains
- Register chains
- Local interconnect

Figure 2–4 shows the LAB structure for Cyclone IV devices.
Cyclone IV Architecture - Embedded Memory

- 66 blocks of 8K (1024) bit SRAM in columns
- RAM, ROM, FIFO, shift register
- One parity bit for each byte
- Fully synchronous SRAM (registered data and address)
- Memory can be preloaded during initialization
- Multiple configurations possible
Cyclone IV Architecture - Embedded Memory

- Memory Configurations

Single Port Memory

- True Dual Port Memory

Simple, Two-Port Memory

Dual-Port FIFO
Cyclone IV Architecture - Embedded Memory

- Memory Configurations - Shift Register Mode
  - Used to implement shift registers for DSP applications
  - Shift register sized by: $width \times tap\_length \times number\_taps$
Cyclone IV (CE22) : 132, 9x9 or 66, 18x18 multipliers
Cascadable for wider operations
Handles signed or unsigned data

Multipliers are in Columns with Adjacent LABs

Multiplier Architecture

Embedded Multiplier Block Overview
Cyclone IV Architecture - I/O

- Comprehensive support: 3.3v, 2.5v, 1.8V, 1.5V, 1.2V, LVDS, LVPECL
- Bidirectional I/O Buffer + Five Registers
- Single-ended or Differential Drive, On Chip Termination, Slew Rate

Figure 6–1 shows the Cyclone IV devices IOE structure for single data rate (SDR) operation.

I/O Element Features

The Cyclone IV IOE offers a range of programmable features for an I/O pin. These features increase the flexibility of I/O utilization and provide a way to reduce the usage of external discrete components, such as pull-up resistors and diodes.

Programmable Current Strength

The output buffer for each Cyclone IV I/O pin has a programmable current strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL-2 Class I and II, SSTL-18 Class I and II, HSTL-18 Class I and II, HSTL-15 Class I and II, and HSTL-12 Class I and II I/O standards have several levels of current strength that you can control.

Note to Figure 6–1: (1) Tri-state control is not available for outputs configured with true differential I/O standards.