

DIRECT DIGITAL SYNTHESIZERS ARE KNOWN FOR THEIR HIGHLY ACCURATE DIGITAL TUNING, LOW NOISE FIGURE, AND PHASE-CONTINUOUS FREQUENCY-HOPPING CAPABILITIES, WHICH MAKE THEM MORE ATTRACTIVE THAN ALTERNATIVE ANALOG FREQUENCY-SYNTHESIS SOLUTIONS.

DDS design

YOU FIND DDSs (direct digital synthesizers) in applications such as radios, instrumentation, and radar systems. Though large and unpredictable spurious responses have troubled old designs, innovations have improved DDS performance, and the worst-case spurs are now smaller and predictable. Careful frequency planning allows you to place the worst-case spurs outside the bandwidth of interest, so you can easily filter them.

Most DDS applications use only a fraction of their output spectrum and attenuate the remainder with external filters. The bandwidth of interest is typically from 0 Hz to about 40% of the sampling frequency. The sub-Nyquist limitation is due to the transition band of the external image-rejection filter. Some applications can use the image band and eliminate an upconversion stage, but the reduced power in the image lowers the SNR. Image use also requires bandpass filtering rather than a lowpass filter. The DAC's zero-order sample-and-hold imparts a Sinc ($\sin(x)/x$) attenuation envelope to the fundamental, images, and harmonics in the DDS spectrum.

A DDS has four principal spur sources: the reference clock, truncation in the phase accumulator, angle-to-amplitude mapping errors, and DAC error terms, including nonlinearities and quantization noise (Figure 1). The spur frequencies' predictability allows you to develop an effective frequency plan.

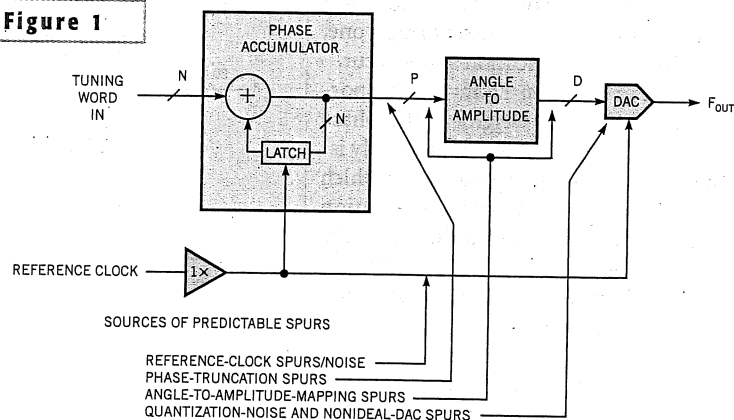
REFERENCE CLOCK

A DDS functions like a high-resolution frequency divider with the reference clock as its input and the DAC as its output. The spectral characteristics of the reference clock directly impact those of the output. Though phase noise and spurs on the reference clock also appear at the DAC output, they do so at a reduced magnitude due to the frequency division. The improvement, expressed in decibels, is $20 \log(N)$, where N is the ratio of input to output frequencies. For example, two trials dividing a 300-MHz clock down to 80 and 5 MHz result in a dif-

ference in their phase-noise plots of $20 \log(16) = 24$ dB (Figure 2). The DDS's internal reference-clock path is the dominant contributor of phase noise from the DDS.

Modulating the clock amplitude generates spurs in its output spectrum. A 400-MHz RF carrier with 10% AM (amplitude modulation) by a 100-kHz sine-wave signal demonstrates the effect you see at the reference clock and 10.119-MHz DDS outputs (Figure 3). The figure, which superimposes the reference-clock and DAC-output spectra, shows the amplitude reduction in AM clock spurs at the DDS output. The attenuation calculation, $20 \log(400 \text{ MHz}/10.119 \text{ MHz})$, predicts a 32-dB improvement, although the plot shows more. The additional spur attenuation is due to the fact that the modulated sine wave of the reference-clock signal encounters a limiter or squaring circuit at the DDS input. The limiter stage converts the sine wave to a square wave, and the AM spurs are thus converted to PM (phase modulation) spurs. The AM-to-PM conversion results in an additional attenuation of spurs that depends on the characteristics of the limiter circuit but is typically on the order of -6 dB.

Figure 1



A DDS has four principal sources of spurs.

The quality of the reference clock imposes limits on DDS performance in ways that are often recognizable. The reference clock usually causes those DDS spurs that maintain their relationship to the carrier as you change the output frequency. Also, there is some degree of noise at the input of any circuit. A high-slew-rate reference clock spends less time traversing the region where noise can cause jitter.

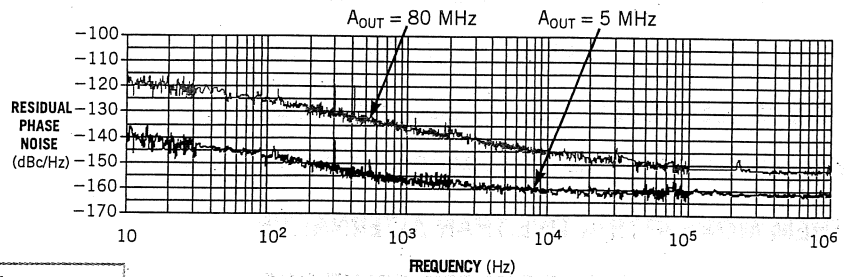
PHASE TRUNCATION

Consider a DDS with a 32-bit phase accumulator. If the design maintained all 32 bits throughout, the DDS core would occupy a large die area and dissipate significant power. Truncating the value from the phase accumulator—that is, passing only the accumulator's most significant bits to the angle-to-amplitude mapper—reduces the power dissipation and die area as well as the phase resolution of the angle-to-amplitude mapper.

The DDS's phase-truncation spur mechanism models as a noise source summed with an otherwise-ideal synthesizer (Figure 4). The example truncates a 20-bit phase accumulator to 8 bits. T is the phase accumulator's tuning-word width. Each update of the reference clock adds the value of T to the accumulator output. The output is divided into two sections, the truncated phase word, P, which is sent to the mapper, and the discarded bits, $M = T - P$. As the value in the discarded section accumulates, it eventually overflows into the truncated phase word. One effect of this overflow is production of phase-modulation spurs. A second effect is that those overflows maintain the full-frequency resolution of T. Note, if no bits in the discarded portion are set to logic one, then no phase-truncation spurs occur.

Phase-truncation spurs are proportional to the LSB weight in the phase word and, therefore, are not typically issues. Conversely, in applications in which a DDS drives a PLL, phase-truncation spurs within the loop bandwidth of the PLL will be amplified by $20 \log(N)$ dB, where N is the PLL-multiplication factor. The accumulator's phase-word output should be 3 or more bits wider than the DAC resolution suggests. You can calculate the worst-case spurious magnitude attributable to the phase-word width as $-6.02P$.

Figure 2



Increasing a 300-MHz reference clock's divisor reduces but does not eliminate the reference clock's contribution to the output phase noise.

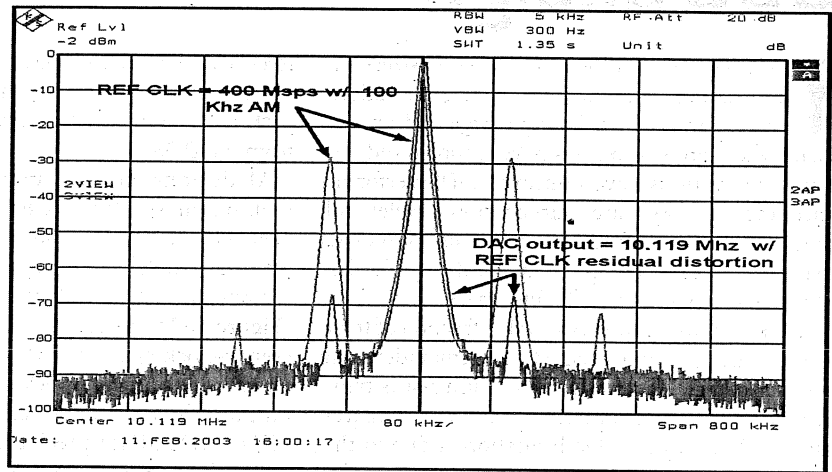


Figure 3

Spurs caused by modulation of the reference-clock amplitude are also reduced by $20 \log(N)$. The DDS's input limiter, which converts the amplitude modulation into a phase-modulation term, provides additional suppression of this spur.

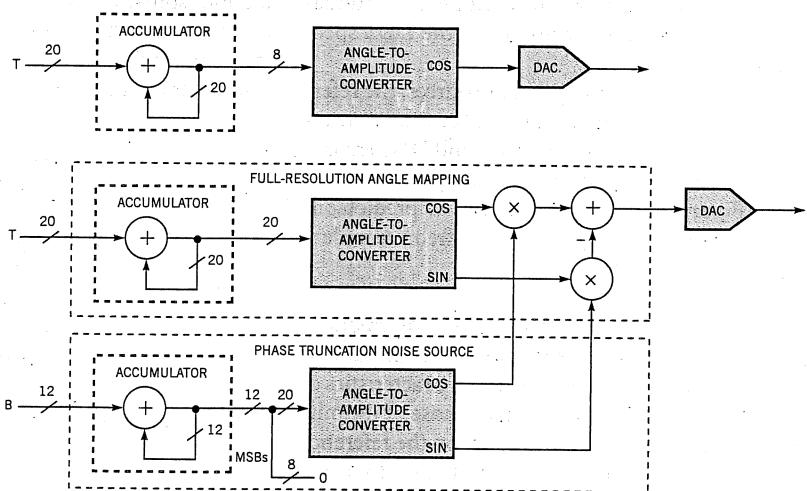


Figure 4

The DDS's phase-truncation spur mechanism models as a noise source summed with an otherwise-ideal synthesizer.

dBc, where P is the number of bits in the phase word. So, a 12- to 19-bit phase resolution produces a -72- to -114-dBc spurious magnitude.

The tuning-word width, its fraction disposed of through truncation, and the reference-clock frequency combine to reveal the frequency offset of the truncation-spur phase-modulated sidebands.

$$f_s = f_{REF} \frac{M}{2^N}, \quad (1)$$

where f_s is the spur offset frequency, f_{REF} is the reference-clock output frequency, M is the decimal value of the discarded bits, and N is the number of discarded bits.

These sidebands appear on both sides of the fundamental. If the offset frequency is greater than the output frequency or greater than the difference between the output and the Nyquist frequencies, the sidebands fold around dc, Nyquist, or both.

Figure 5 shows phase-truncation spurs that were generated from a DDS with 14-bit phase resolution and a 32-bit tuning word. The first phase-truncation sideband spurs are approximately -84 dBc, as you would expect from the equation -6.02P. Here, the phase word is 4 bits above the DAC resolution of 10 bits. A 19-bit phase word would place the theoretical magnitudes of phase-truncation spurs at around -114 dBc.

ANGLE-TO-AMPLITUDE MAPPING

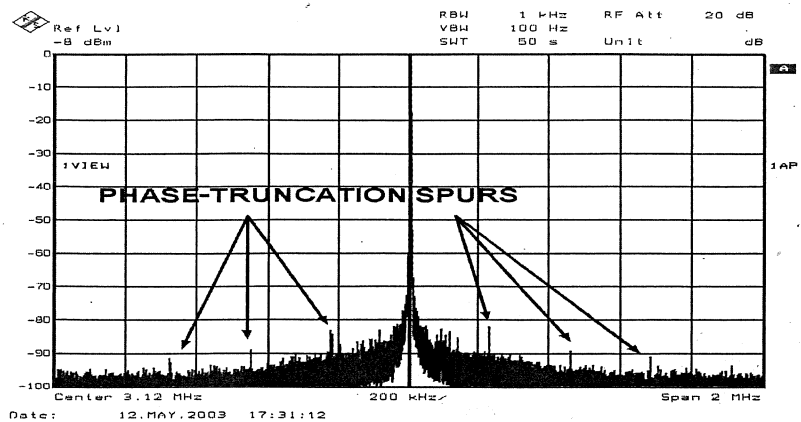
DDS designs can implement the phase-to-amplitude block algorithmically—which reduces die area and power consumption—or as a ROM look-up table. The algorithmic approach enhances hardware efficiency, but its approximations may generate higher spur levels.

The phase-to-amplitude conversion of a time-sampled sine wave is

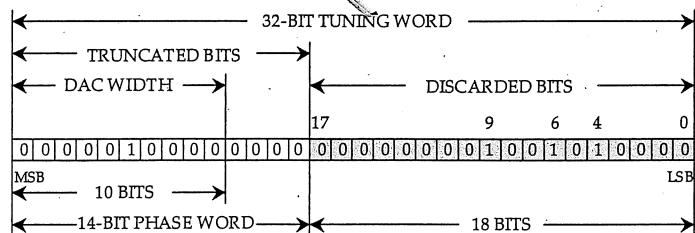
$$V_{a_i} = V_p \sin(\phi_i), \quad (2)$$

where V_{a_i} is the sample amplitude, V_p is half of the DAC's full-scale voltage, and ϕ_i is the value of the sample's phase word.

It's unlikely that the V_{a_i} that the system calculates corresponds exactly to a DAC code, so the DDS selects the nearest code, resulting in a residual error. If the phase word has too few bits, the V_{a_i} calculation may skip over DAC codes (Figure 6).



(a)



$$\text{PHASE-TRUNCATION SPUR SPACING} = \frac{\text{DECIMAL EQUIVALENT OF DISCARDED BITS}}{2^{\text{NUMBER OF DISCARDED BITS}}} \times$$

$$f_{REF} = \frac{2^9 + 2^6 + 2^4}{2^{18}} \times 100\text{M SAMPLES/SEC} = 266 \text{ kHz.} \quad (b)$$

Figure 5

The phase-truncation spurs are offset from the fundamental by 266 kHz and its harmonics (a). The reference-clock rate and analyzing the 32-bit tuning word reveal this fact. The calculation shows how to predict the 266-kHz spur spacing (b).

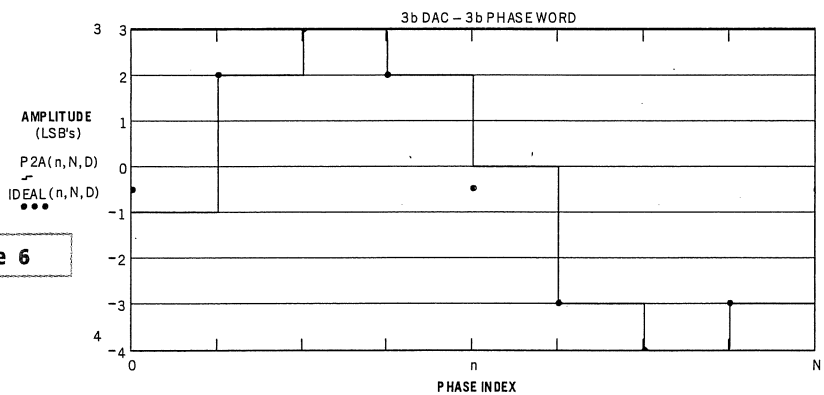


Figure 6

Limited phase resolution results in skipping DAC codes. The blue circles at each phase increment show the calculated V_{a_i} .

Conversely, retaining more bits in the phase word reduces these errors (Figure 7). To guarantee that all DAC codes are available to the phase-to-amplitude converter, a good rule of thumb is to set the phase word to a minimum of 3 bits wider

than the DAC. The red trace in Figure 7 represents the amplitude error signal resulting from the DAC's finite resolution. It indicates the difference between V_{a_i} and the actual DAC codes. A Fourier transform of this time-domain plot

would display a corresponding spectral plot with discernible frequency spurs. You can interpret the error as a modulating signal acting on the sine wave (blue trace). You can determine the resulting spurs' frequency locations and approximate their amplitudes, although the amplitudes are subject to some architectural dependencies. In some DDSs, the amplitude of the worst-case spurs ranges from -12 to -24 dB below the DAC-quantization-noise level. The quantization noise (SNR) is proportional to the DAC resolution:

$$\text{SNR} = 6.02N + 1.76 \text{ (dB)}, \quad (3)$$

where N is the DAC resolution in bits.

A normalized spectral plot of a simulated look-up-table based DDS displays the spurious response that the amplitude-error signal causes (Figure 8). The plot includes no DAC-error effects. The DDS tuning word is 32 bits, the phase word is 19 bits, the reference clock is 100M samples/sec, and the DAC resolution is 10 bits. The tuning word is 30002000H, which results in a carrier fre-

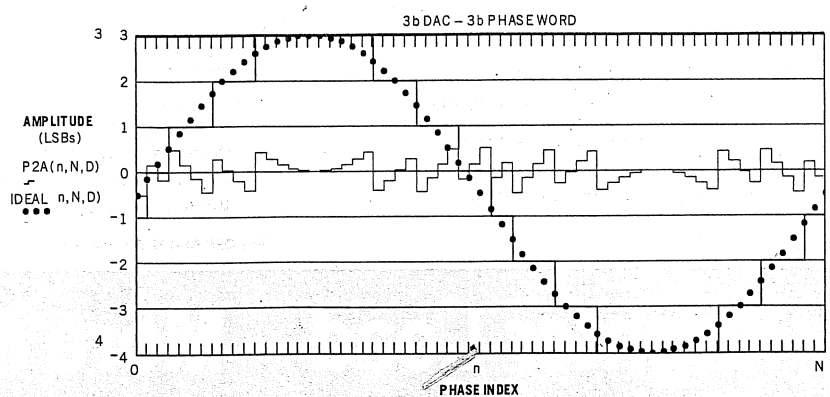


Figure 7

Adding three phase bits increases the phase resolution and takes advantage of the DAC's full dynamic range.

quency of 18.75021876 MHz. The staircase spectrum results from the amplitude-error signal modulating the carrier. The dominant, or worst-case, spurs are offset approximately ± 700 kHz from the carrier with this tuning word. Their location depends on the tuning word and the DDS architecture. Their power level

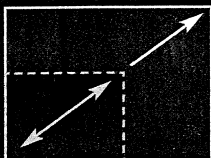
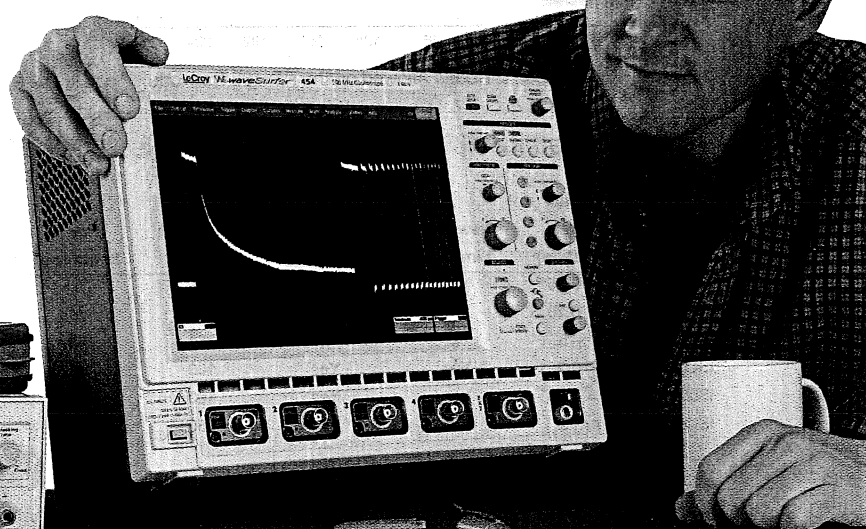
is below the DAC's expected SNR, which is a goal of the design. A DAC with greater resolution would decrease the magnitudes of these spurs. A similar DDS implemented with an algorithmic sine mapper instead of the ROM-based structure produces a similar spectrum (Figure 9).

EXPECT TO MAKE WAVES.

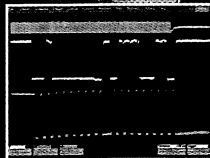
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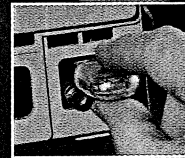
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Instead of performing a Fourier transform of the amplitude-error signal, a relatively simple method determines the frequency of the most prominent spurs for a given tuning word. This method uses a test tuning word with only one bit set. The resulting spectrum consists of the test carrier and its spurs, the offsets and spacings of which harmonically relate to the carrier frequency. The spectral region where these spurs reside is

$$f_s = f_{REF} \frac{\pi}{2^{b-n}}, \quad (4)$$

where b represents the location of the single bit asserted in the tuning word, and n is the DAC resolution in bits. This analysis method proceeds through nine steps:

1. Accurately measure and record the reference-clock frequency, f_{REF} , to a ± 1 -Hz tolerance.

2. Counting from the MSB of the tuning word, assert only the b th bit. The b th bit is defined as $b \geq n + 8$; that is, if the DAC width is 10 bits, then set 18th bit or

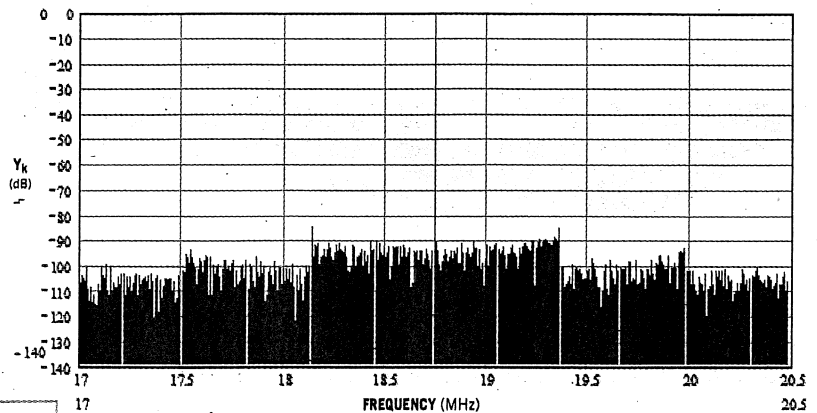


Figure 8

An FFT plot of a simulated ROM-based DDS shows DAC-amplitude-error-induced spurs.

higher counting from the MSB.

3. Calculate the tuning-word frequency, f_C , from f_{REF} and the tuning word.

4. Use Equation 4 to locate the frequency region of the prominent spur set to measure. Note that the spacing between these sets of spurs is two times

the tuning-word frequency.

5. Measure and record the frequency of each individual spur in the worst-case set.

6. Individually divide the frequencies of the worst-case spur set by the tuning word. Round the results to the nearest

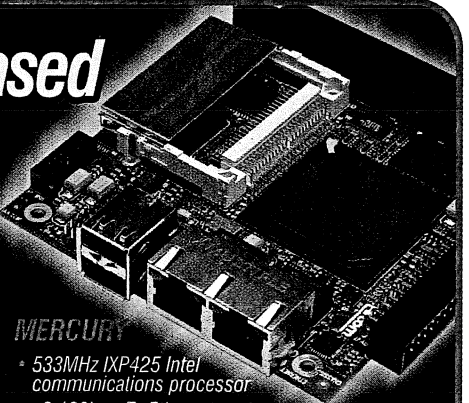
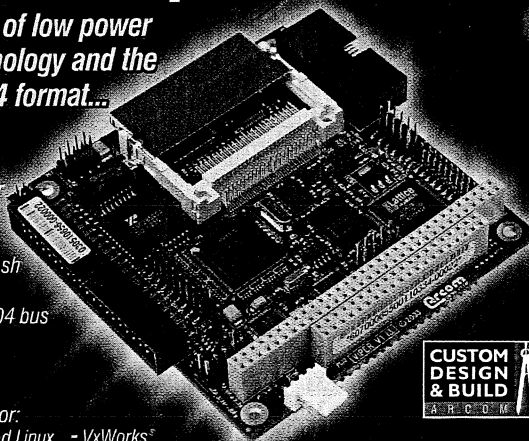
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whole number. The results will probably be consecutive odd numbers.

7. These results of Step 6 are harmonically related to the tuning word. When you change the tuning word, predict the locations of the corresponding spurs by multiplying the new tuning word by each value in Step 6.

8. Terms from Step 7 greater than Nyquist, $f_{REF}/2$ will alias. To locate the alias if the product is above Nyquist but below f_{REF} , subtract the f_{REF} from the product; the difference is where the alias resides. To locate the alias if the product

is above f_{REF} , divide by f_{REF} and analyze the remainder of the quotient. If the remainder is below 0.5, multiply it by f_{REF} . Otherwise, subtract it from 1 and then multiply by f_{REF} .

9. Repeat steps 7 and 8 for every value found in Step 6.

Plots of the AD9850/51 DDS demonstrate how these calculations find the worst-case angle-to-amplitude spurs as a function of the tuning word. In this case, the f_{REF} is 100 MHz (Figure 10). The tuning word has only the 18th bit set from the MSB in the top plot and is

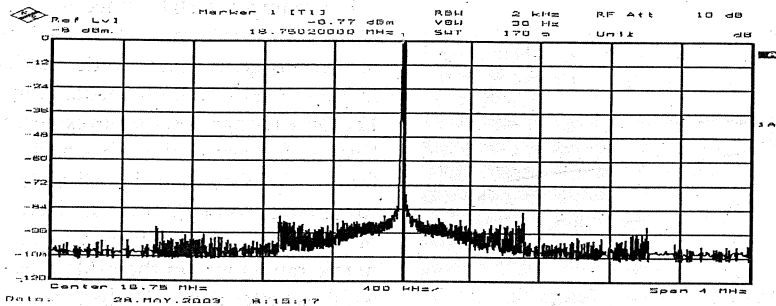


Figure 9

A similar DDS implemented with an algorithmic sine mapper instead of the ROM-based structure in Figure 8 produces a similar spectrum. Note that the worst-case spurs have the same frequency offset.

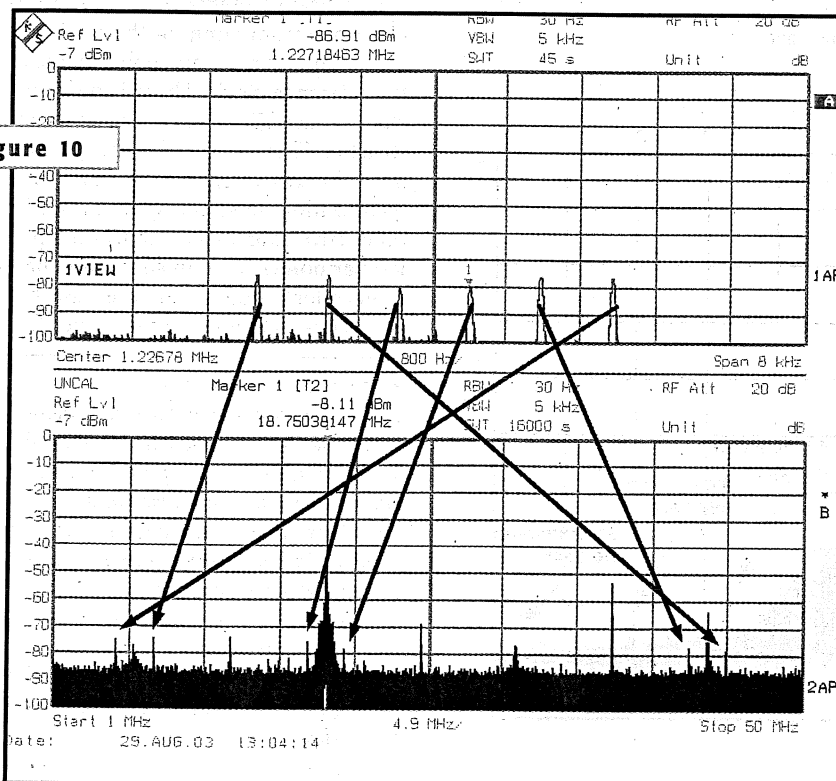
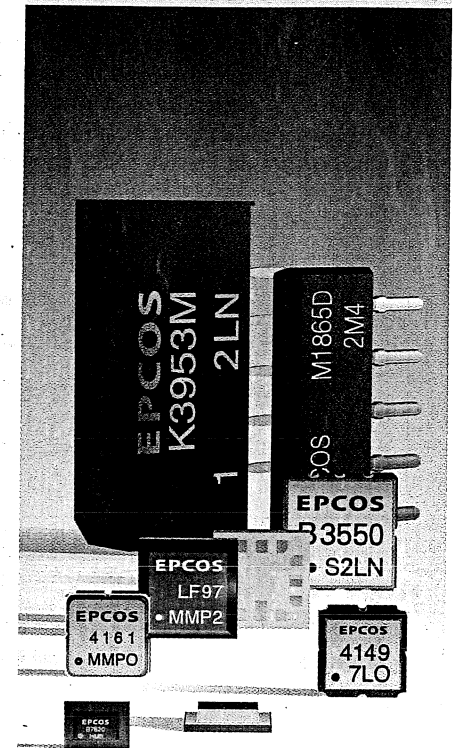
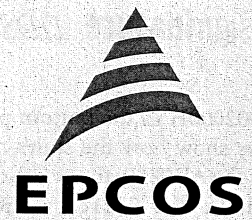


Figure 10

Spurs keep their harmonic relationship to carrier changes.

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30002000H in the bottom plot. The arrows show how the spurs redistribute. For the AD9850, the worst-case spur set includes the 3211th, 3213th, 3215th, 3217th, 3219th, 3221th harmonics of the tuning word.

QUANTIZATION NOISE, DAC NONLINEARITIES

A DAC's quantization noise and distortion determine its SNR. You can calculate a first-order approximation of SNR by taking the ratio between the quantization-noise power, integrated over the Nyquist bandwidth, and the power in the fundamental. As a result, SNR is propor-

tional to the DAC resolution in bits, as given in Equation 3. This SNR calculation describes an ideal DAC. Real DACs also have nonlinearities due to process mismatches and imperfect bit-weight scaling. Nonideal switching characteristics also add distortion and nonlinearity.

The most prominent DAC spurs are usually due to nonideal switching characteristics, which, along with any nonlinearity in the transfer function, appear as lower order harmonics of the fundamental. Both quantization noise and the nonideal DAC properties produce a response that consists of harmonically re-

lated spurs of the fundamental. This relationship is the key to understanding how to predict the frequency location of the prominent spurs.

Harmonics alias because the DAC is a time-sampled system. As a result, the carrier's harmonics, the reference clock, and the reference clock's harmonics create numerous sum- and difference-mixing products. The well-defined mathematical relationship of these products makes predicting the spur locations possible. Harmonics beyond the first Nyquist zone are mapped back to the first Nyquist zone (Figure 11).

For example, a DDS tuned to 25.153 MHz with a reference clock of 100M samples/sec generates low-order odd harmonics close to the fundamental (Figure 12). Once the harmonic series exceeds the Nyquist frequency, they alias back into the first Nyquist zone in a predictable way (difference product). This DDS has a 14-bit DAC. The SFDR (spurious-free dynamic range) within the 4-MHz bandwidth is better than -73 dBc. Increased oversampling—by raising f_{REF} to 400M samples/sec—eliminates the alias products of the third, fifth, and seventh harmonics within the first Nyquist zone.

Significant benefits arise in DDS applications from running the DDS and comparator at a simple subharmonic of the reference clock. These benefits include reduced jitter and a simpler reconstruction filter. Because f_{REF} and f_C are related by an integer ratio, the DAC quantization noise and spurs caused by other error sources fall exactly on top of the harmonics of f_C . In such cases, harmonics don't produce jitter, because they are phase-coherent with the carrier. □

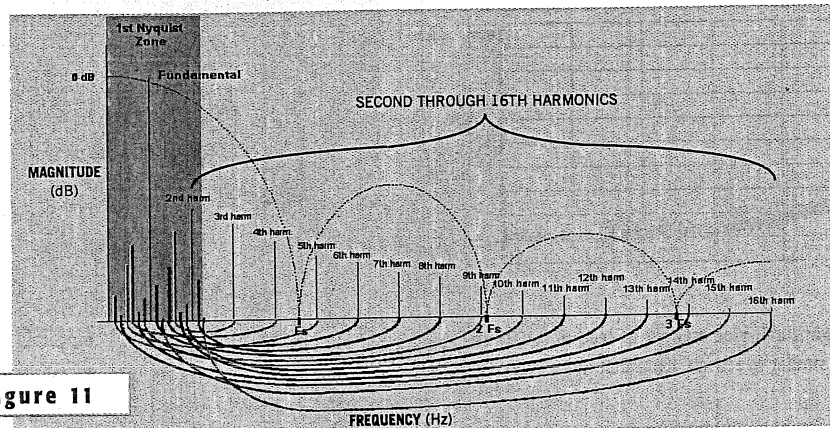


Figure 11

Spur energy beyond f_{REF} also aliases to the first Nyquist zone.

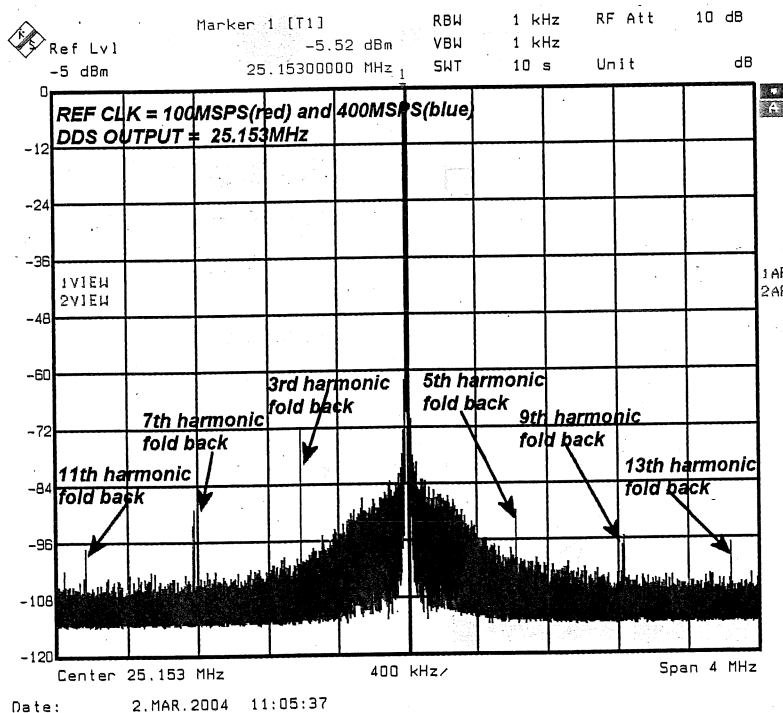


Figure 12

You can eliminate spurs caused by aliases of low-order harmonics (red) by increasing f_{REF} (blue).

AUTHOR'S BIOGRAPHY

David Brandon is an application engineer at Analog Devices, where he is responsible for customer support, application notes, and new-product input. He has an associate's degree in electrical engineering from Guilford Technical Institute and more than 21 years of job experience.

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