ECE 474/574 Design Problem

1.0 Revision History

ver 1.1 4/1/97 - Original version
ver 1.2 4/1/97 - Fixed misspelling and changed temperature spec to 0 to 127.
ver 1.3 4/7/94 - Changed RAM address specification.
ver 1.4 4/11/97 - Changes as follows:

- Changed problem statement so that new readings made on the light/dark border will not be sent until one second after old queued temperature readings are sent.
- Also made allowance for probe to send data in less than one hour to allow garbage packets to be sent.
- Added *reset_n* pin to tas.

2.0 Background

NASA has launched a space probe that is to orbit the moon of a planet in our solar system. This probe, among its other duties, is to report back to earth at 5 to 15 minute intervals the temperature at the surface of the moon.

3.0 Operation

The space probe records four temperature readings per hour. When the probe is in continuous radio contact with tracking stations, a header of either 0xA5 or 0xC3 will be sent followed by four temperature readings, sent no closer than every 5 minutes apart and no further than 15 minutes apart. The temperature averaging system (tas) averages the four readings and writes the result to RAM.

As the probe orbits the moon it will periodically loose contact with earth for up to one hour. (i.e. 1 orbit every 2hrs) During these times, the probe queues the temperature readings until contact is reestablished. Therefore, sometimes partial packets will be received consisting of only a header or a header plus one to three temperature readings. In this case, the packet bytes remain in order and the remaining bytes are sent upon reestablishing contact.

In the case where there are readings queued in the probe and at the moment of radio contact establishment, another temperature reading must be sent, the probe will delay sending the new reading for one second after the old readings are sent.

4.0 Requirements

A digital system is required to capture the temperature information sent from the probe and write the hourly average temperatures into a two-port static RAM (2K x 8) where further processing will take place with the aid of a microcomputer.

The interface of the tas to the outside world is as follows:

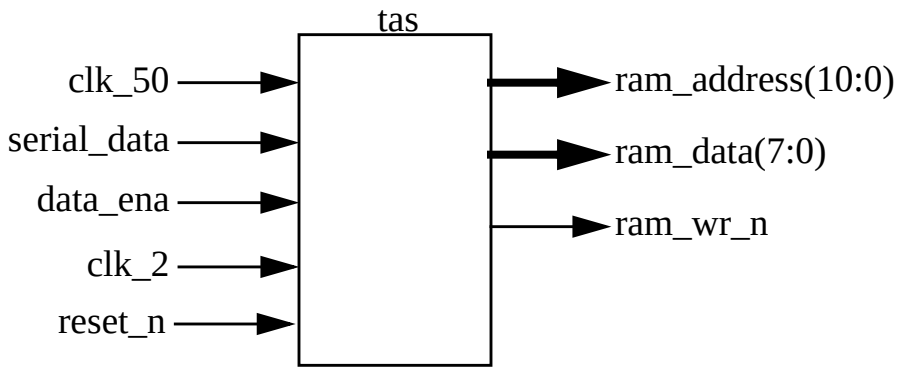

FIGURE 1. Temperature Averaging System Top Level Interface Diagram

4.1 Message Protocol

All data from the probe is sent within a five byte packet. Each packet is preceeded with a header indicating the data type. Four data bytes follow. The header indicating temperature data will be either 0xA5 or 0xC3. Data packets other than temperature data is to be rejected.

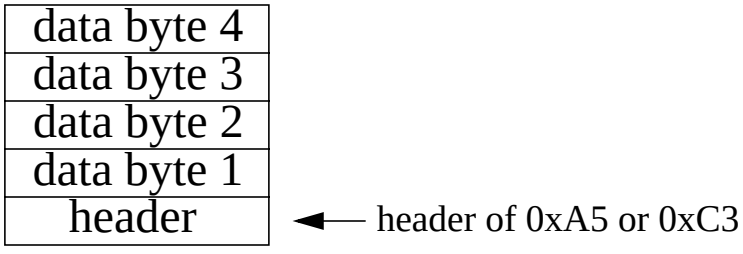

FIGURE 2. Packetized data format

4.2 Data Format

The temperature information in the data fields is in binary format. It will range in value from 0 to 127 to indicate temperature in degrees.

4.3 Input Timing

Data from the probe is sent clock synchronous at a 50Mhz rate. The 50 MHz clock from external logic is free running (i.e. never stops).

The reset signal *reset_n* is asserted early before any clock or enable signals begin to assert. It should be used to reset all your logic.

Bits within a byte are sent consecutively. Consecutive bytes (header or data) are separated by one at least one 50Mhz clock cycle. See timing below.

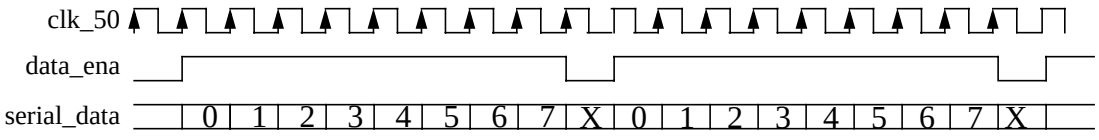

FIGURE 3. Timing of Packets

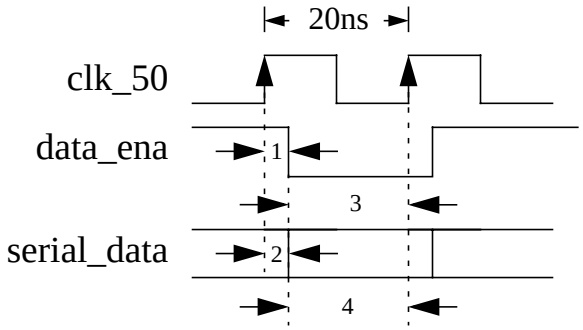

FIGURE 4. Timing Detail for Serial Interface

description	min (ns)	max(ns)
(1) hold time clk_50 to data_ena changing	2	5
(2) hold time clk_50 to serial_data changing	2	5
(3) setup time data_ena valid before rising edge of clk_50	10	15
(4) setup time serial_data valid before rising edge of clk_50	10	15
clock period (50MHz)	20ns	

TABLE 1. Setup and Hold Times for Serial Interface

4.4 Output Data Format

The data written to RAM consists of subsequent averaged temperatures written to RAM starting at address 0x07FF. Subsequent averages are written to the next lower address location; 0x07FE, 0x07FD, etc.When location 0x0000 is written, the next write is to location 0x07FF.

Header bytes are not to be stored in RAM.

4.5 RAM Timing

The averaged temperature data is to be written into an asynchronous static RAM. This RAM is configured as 2K by 8 bits. The system described here needs only control the address, data and a write strobe. The write strobe signal ram_wr_n must be guaranteed to be glitch free and should be asserted for the minimum time allowed by the system. The timing for the RAM is as follows:

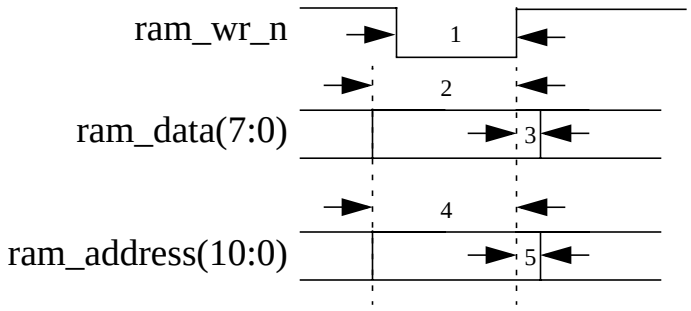

FIGURE 5. RAM Interface Timing Detail

description	min (ns)	max(ns)
(1) pulse width, ram_wr_n	50	
(2) setup time, ram_data valid before ram_wr_n rising	10	
(3) hold time, ram_data after rising edge of ram_wr_n	5	
(4) setup time, ram_address valid before rising edge of ram_wr_n	15	
(5) hold time, ram_address after rising edge of ram_wr_n	5	

TABLE 2. Setup and Hold Times for RAM Interface

4.6 Miscellaneous Requirements

The temperature averaging system is to operate at a clock frequency of 2Mhz where possible.

The maximum number of gates is 1000.

Minimize clock loading to limit power dissipation.(extra credit!?)