Attributes

Attributes specify “extra” information about some aspect of a VHDL model.

There are a number of predefined attributes provide a way to query arrays, bit, and bit vectors.

Additional attributes may be defined by the user.

Format:

```
object_name’attribute_designator
```

The “ ‘ ” is referred to as “tick”.

Example:

```
ELSIF (clk’EVENT AND clk = ‘1’) THEN
```

Predefined Signal Attributes

signal'EVENT - returns value "TRUE" or "FALSE" if event occurred in present delta time period.

signal'ACTIVE - returns value "TRUE" or "FALSE" if activity occurred in present delta time period.

signal'STABLE - returns a signal value "TRUE" or "FALSE" based on event in (t) time units.

signal'QUIET - returns a signal value "TRUE" or "FALSE" based on activity in (t) time units.

signal'TRANSACTION - returns an event whenever there is activity on the signal.

signal'DELAYED(t) - returns a signal delayed (t) time units.

signal'LAST_EVENT - returns amount of time since last event.

signal'LAST_ACTIVE - returns amount of time since last activity.

signal'LAST_VALUE - returns value equal to previous value.

Using Attributes

Rising clock edge:

```
clk'EVENT and clk = '1'
```

OR:

```
NOT clk'STABLE AND clk ='1'
```

Falling clock edge:

```
clk'EVENT AND clk = '0'
```

Checking for too short pulse width:

```
ASSERT (reset'LAST_EVENT >= 3ns)
  REPORT "reset pulse too short!";
```

Checking stability of a signal:

```
signal'STABLE(10ns)
```