Running VSIM

The Simulator

The simulator we will be using is the Model Technologies' *ModelSim*. It will be referred to as *vsim*. Vsim is a full featured VHDL and/or Verilog simulator with best-in-class VHDL simulation. It is also very easy to learn and use.

VHDL Libraries

Before a VHDL design can be simulated, it must be compiled into a machine executable form. The compiled image is placed into a library where the simulator expects to find the executable image. Therefore we must first create a special directory called "work".

The Library *work*

The library named work has special attributes within vsim; it is predefined in the compiler. It is also the library name used by the compiler as the default destination of compiled design units. In other words the work library is the working library.

Creating *work*

At the desired location in your directory tree, type:

```
vlib work
```

You will see a directory work created. You cannot create work with the UNIX *mkdir* command.

Compile the code

Suppose our example code is in a file called *aoi4.vhd*. At the level at which you can see the directory *work* with an *ls* command, simply type:

```
vcom -93 aoi4.vhd
```

Then you will see:

```
brilthor.ECE.ORST.EDU:vcom -93 src/aoi4.vhd
Model Technology ModelSim SE/EE vcom 5.4c Compiler 2000.08 Jul 29 2000
-- Loading package standard
-- Loading package std_logic_1164
-- Compiling entity aoi4
-- Compiling architecture data_flow of aoi4
brilthor.ECE.ORST.EDU:
```

If you look in the work directory, you will see a subdirectory in work with the entity name *aoi4*. In there are the files necessary to simulate the design.

With a clean compilation, we are ready to simulate.

Simulate the design

Invoke the simulator by typing *vsim* at the UNIX prompt. You will see the *Load Design* window open over the main *vsim* window.
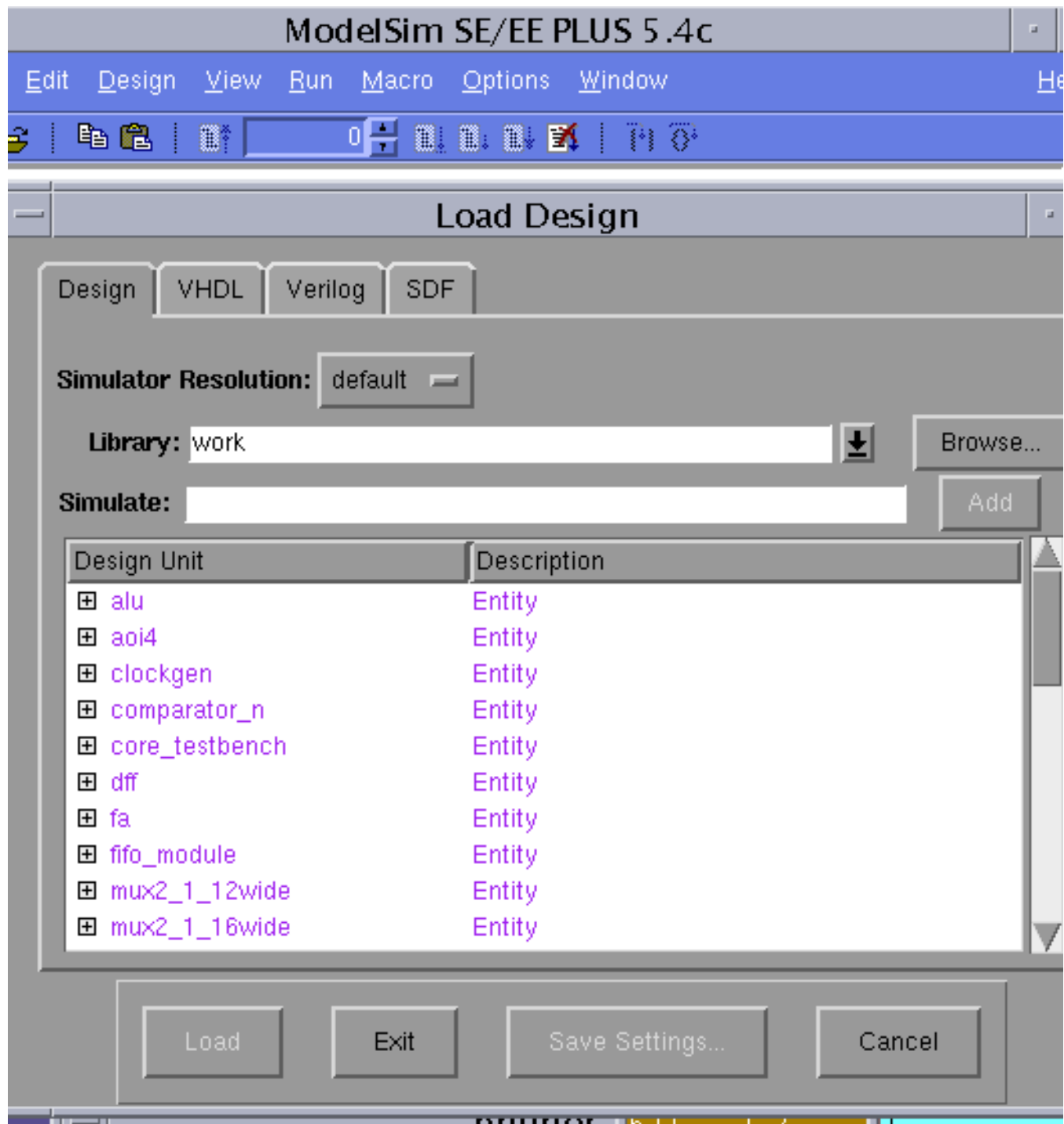
The *Design Unit* is the name of the entity you want to load into the simulator. In this example, there are many other entities in the work directory, each corresponding to a different entity/architecture pair.

To load the design, click on *aoi4* and then *Load*. Note that *aoi4* this is not the file name, but the entity name.

The design will then load. To run a simulation, first type view * in the ModelSim window. This will open all the windows available for the simulation. You will probably want to close all but the wave, signals, source and structure windows.

To observe the signals, in the *Signals* window select:
**View > Wave > Signals in Region**
All the signals in the design are then visible in the Wave window.

To provide stimulation to our model we can just force the input signals and run for a short time. To do this, in the ModelSim window we can type:

```
force a 0
force b 0
force c 0
force d 0
run 100
force a 1
force b 1
run 100
```

According to our model we should see the z output assert to a zero when either a and b or c and d both become true. We can see the correct behavior in the wave window.

The output from the wave window looks like this:
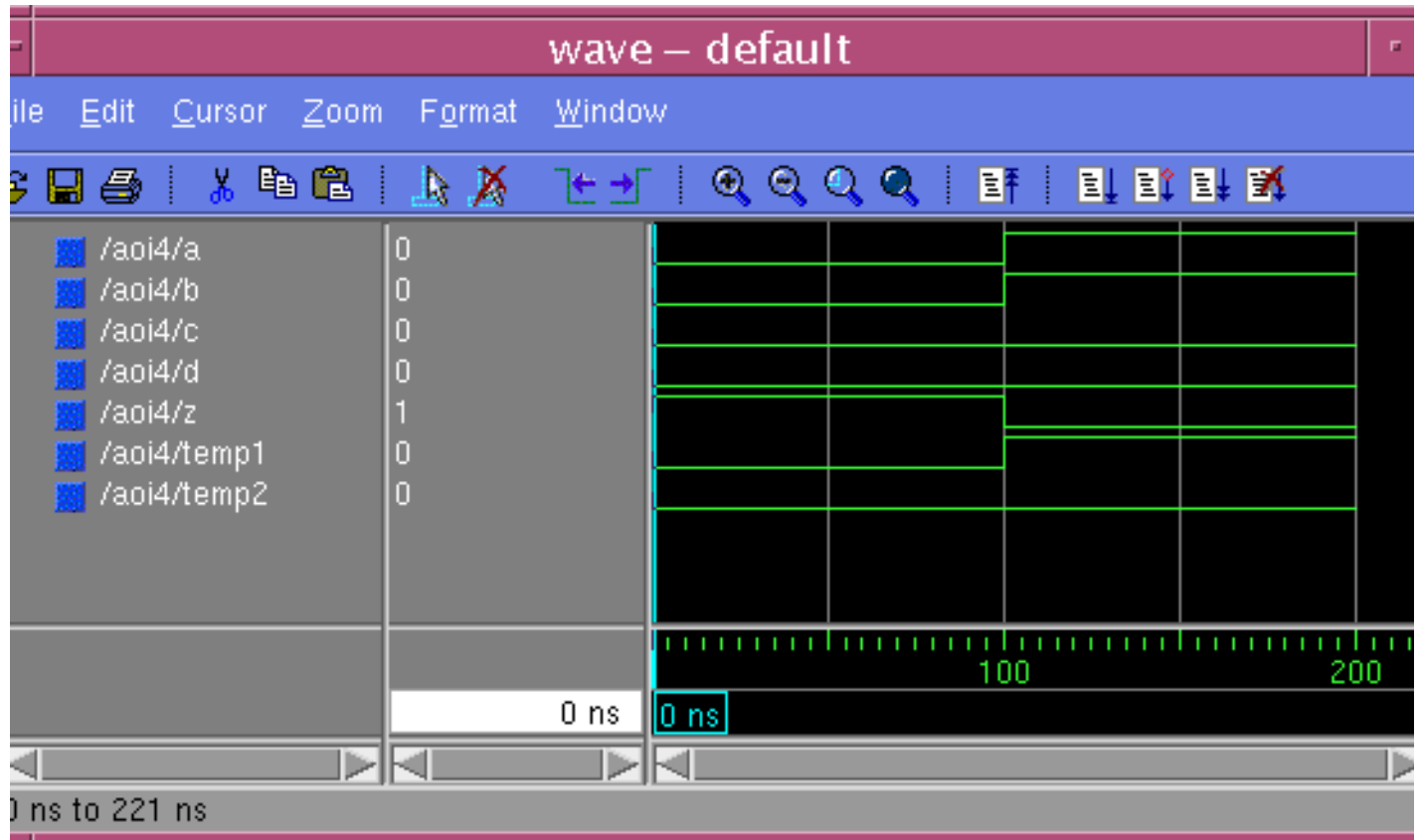
We will make heavy usage of the *vsim* simulator. You are encouraged to explore and discover the different options and way to operate the simulator.

For example, the force commands may be applied from a "do file". This is a text file containing all the force and run commands. Try to use a force file to exhaustively test the aoi4 design.

The documentation for the Model Technology tools may be found within the tool by using the Help pulldown menu.