# Sequential Operations

**Statements within processes are executed in the order in which they are written.**

**The sequential statements we will look at are:**

- **Variable Assignment**
- **Signal Assignment***
- **If Statement**
- **Case Statement**
- **Loops**
- **Next Statement**
- **Exit Statement**
- **Return Statement**
- **Null Statement**
- **Procedure Call**
- **Assertion Statement***

***Have both a sequential and concurrent form.**

# Variable Declaration and Assignment

**Variables can be used only within sequential areas.**

**Format:**

```
VARIABLE var_name : type [:= initial_value];
```

**Example:**

```
VARIABLE spam  : std_logic := ‘0’;


ARCHITECTURE example OF funny_gate IS
SIGNAL c : STD_LOGIC;
  BEGIN
    funny: PROCESS (a,b,c)
    VARIABLE temp  : std_logic;
    BEGIN
      temp := a AND b;
      z <= temp OR c;
    END PROCESS funny;
 END ARCHITECTURE example;
```

**Variables assume value instantly.**

**Variables simulate more quickly since they have no time dimension.**

**Remember, variables and signals have different assignment operators:**

```
a <= new_value;  --signal assignment
a := new_value; --variable assignment
```