Text I/O

One of the predefined packages n the STD library that is supplied with VHDL is “TEXTIO” It may be accessed if you include the statement:

```
USE STD.TEXTIO.ALL;
```

This package contains procedures and functions that provide the ability to read and write ASCII text files.

TEXTIO considers files to be files of lines, where a line is a carriage return terminated text string.

The package defines a number of types that can be used with text files. A variable of type LINE is defined to hold a line of text. The line is the basic unit upon which TEXTIO operates. For example, to read a set of values from a file, the line is first read, and then the individual elements of the line. The TEXTIO package provides the necessary functions to do this.

Procedures most commonly used:

```
endfile(file_name)
--returns boolean true is the end of file is reached


readline(input_file_name, input_line_variable)
--reads a new line into the line variable from the input file


writeline(output_file_name, output_line_variable)
--writes a new line from the line variable to the output file


read(input_line_variable, variable_read)
--reads the next available variable from the line

write(output_line_variable, variable_to_write)
--writes an new variable into the line
```

Here is an example of how these can be used:

```
LIBRARY IEEE,STD;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_TEXTIO.ALL;
USE STD.TEXTIO.ALL;

ENTITY text_io_example IS
END text_io_example;

ARCHITECTURE beh OF text_io_example IS
BEGIN

file_io:
PROCESS IS
  FILE in_file          : TEXT OPEN READ_MODE  IS "in_values";
  FILE out_file         : TEXT OPEN WRITE_MODE IS "out_values";
  VARIABLE out_line     : LINE;
  VARIABLE in_line      : LINE;
  VARIABLE a,b,c        : STD_LOGIC;
  BEGIN
    WHILE NOT ENDFILE(in_file) LOOP --do this till out of data
      READLINE(in_file, in_line);      --get line of input stimulus
      READ(in_line, a);                --get first operand
      READ(in_line, b);                --get second operand
      c := a AND b;                    --operate on the data
      WRITE(out_line, c);              --save results to line
      WRITELINE(out_file, out_line);   --write line to file
  END LOOP;
  ASSERT FALSE REPORT "Simulation done" SEVERITY NOTE;
  WAIT;  --allows the simulation to halt!
END PROCESS;
END beh;
```

Here are the input and resultant out files:

“in_values”	outvalues
0 0	0
1 0	0
0 1	0
1 1	1

Note the inclusion of **`IEEE.STD_LOGIC_TEXTIO.ALL`**. This library overloads the definitions in TEXTIO for std_logic and std_logic_vector types.