Fully Embedded Board-Level Optical Interconnects From Waveguide Fabrication to Device Integration

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***Abstract*—This paper presents the latest progress toward fully embedded board-level optical interconnects in the aspect of waveguide fabrication and device integration. A one-step pattern transfer method is used to form a large cross-section multimode waveguide array with 45° micromirrors by silicon hard molding method. Optimized by a novel spin-coating surface smoothing method for the master mold, the waveguide propagation loss is reduced to 0.09 dB/cm. The coupling efficiency of the metal-coated reflecting mirror, which is embedded in the thin-film waveguide, is simulated by an M^2 factor revised Gaussian beam method and is experimentally measured to be 85%. The active optoelectronic devices, vertical surface emitter lasers and p-i-n photodiodes, are integrated with the mirror-ended waveguide array and successfully demonstrate a 10 Gbps signal transmission over the embeddable optical layer.**

***Index Terms*—45° micromirrors, hard molding, optical interconnects, optical printed circuit board, polymer waveguide, ultraviolet embossing.**

I. Introduction

THE speed and complexity of integrated circuits are increasing rapidly as integrated circuit technology advances from very-large-scale integrated circuits to ultra-large-scale integrated circuits. The number of devices per chip, the number of chips per board, the modulation speed, and the degree of integration continue to increase. The International Technology Roadmap for Semiconductors expects that on-chip local clock speed will constantly increase to 10 GHz by the year 2011[1]. The backplane frequency will boost proportionally to meet the interconnection requirement. The third-generation I/O protocol called peripheral component interconnect (PCI) Express, developed by the Signal Interest Group (SIG) consortium, is becoming an industry standard [2]. PCI Express is expected to increase transfer rates up to 10 GHz in the next seven to ten years. Above the frequency of several gigahertz, copper interconnects on printed circuit board (PCB) made of various dielectric substrates become bandwidth limited due to losses such as the skin effect in the conductors and the dielectric loss from the substrate material. It has been reported that replacing the flame-resistant 4 (FR4) material with newer laminates such as Rogers 4000 can extend the bandwidth of electrical interconnects from 3 to 7.7 GHz but increase the cost by five times [3]. Besides the cost issue, several much worse situations for electrical interconnects are introduced by the unsolvable frequency dependent loss, reflection, and crosstalk.

Optical solutions, which are widely agreed as a better alternative to upgrade the system performance, have been proposed for the upcoming electrical interconnect bottleneck for more than 20 years [4]. Optical interconnects preponderate over the copper links in immunity to electromagnetic interference, independency to impedance mismatch, high-speed operation, and less power consumption beyond some threshold distance [3], [5]. Many optical interconnects schemes have been proposed and investigated, including free space [6], embedded fiber connection [7], and optical slots [8]. However, a seamless interface with electrical components is required from the system packaging point of view. For example, the board-level optical interconnections reported in [6] piled up lasers, detectors, and microlenses on the surface of a PCB. The difficulties regarding packaging, multilayer technology, and reliability still remain to be solved.

We previously introduced a fully embedded board-level optical interconnects to relieve the packaging difficulty [9]. Later on, another paper was published to describe the fabrication of flexible optical waveguides, thermal management of embedded thin-film vertical surface emitter lasers (VCSELs), and optical layer integration with VCSELs and photodiode arrays [10]. In this paper, the latest progress to fulfill the fully embedded architecture is presented. An improved fabrication procedure of a large cross-section multimode waveguide array with 45° micromirrors by one-step pattern transfer method is presented. Low propagation loss waveguides as well as high coupling efficiency micromirrors are experimentally obtained and measured, using a new fabrication process in contrast to [9]. The active optoelectronic devices, VCSELs and p-i-n photodiodes, are integrated with the mirror-ended waveguide array and successfully demonstrate a 10 Gbps signal transmission over the embeddable optical layer.

II. Fully Embedded Board-Level Optical Interconnects

The architecture of the fully embedded optical layer includes a VCSEL array, a p-i-n photodiode array, and a polymeric channel waveguide array with 45° micromirrors functioning as a physical layer of optical interconnection. The driving electrical signals to modulate the VCSELs and the demodulated signals received at the photodiode flow through electrical vias

Manuscript received February 27, 2007; revised April 20, 2007. The work was supported by the National Science Foundation.

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Digital Object Identifier 10.1109/JLT.2007.911115

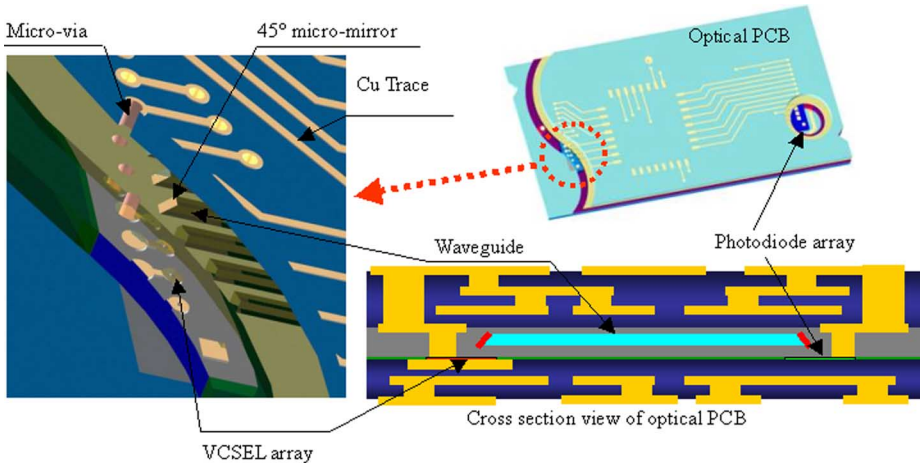

Fig. 1. Illustration of the fully embedded optical interconnect architecture.

connecting to the surface of the PC board, as seen in Fig. 1. Within the optical interconnect layer, the light from the VCSELs is coupled into/out of the waveguide through 45° micromirror couplers and propagates in the polymer waveguide. The fully embedded structure makes the insertion of optoelectronic components into microelectronic systems much more realistic when considering the fact that the major stumbling block for implementing optical interconnection onto high-performance microelectronics is the packaging incompatibility.

To fulfill the embedded structure, two major stumbling blocks need to be solved. A low cost, high performance optical layer on a polymer thin-film represents the first. Packaging the optical layer through via holes and laminating it inside PCB layers stands for the second. The research work presented herein will relieve the concerns for the first major block and is believed to be able to accelerate the deployment of the fully embedded optical interconnect architecture based on the approach in Section V with further efforts.

III. UV Embossed Waveguide Array by Silicon Hard Mold

We previously demonstrated a soft-molded waveguide layer with 45° coupling mirrors that is suitable for the embedded structure [11]. Soft molding method utilizes properly shaped flexible molds—often made of elastomeric polydimethylsiloxane (PDMS) for pattern transfer. Although cheap and easy for fabrication, the soft-molding method still faces serious problems such as durability and size precision. Due to its low Young's module, the soft mold will deform even under a small pressure, resulting in a reduced channel depth and enlarged pitch distance. This expanded pitch will cause the waveguide alignment difficulty with the VCSELs and photodiode array, resulting in increased coupling loss. These shortages can be overcome by replacing the soft-mold material with silicon-based hard mold. Although the silicon master mold, fabricated by photolithography and deep reactive ion etching (DRIE) method, is more expensive than the PDMS soft mold, the production cost per waveguide array is still cheaper than soft-molding method when considering its long durability.

The surface roughness of the silicon master mold directly affects the quality of the molded thin-film waveguide. The high etching rate ($> 1\,\mu\mathrm{m}/\,\mathrm{min}$) and the alternating etching-passivation step in the DRIE process leave silicon sidewalls with coarse and corrugated surfaces. The roughness will be transferred to the polymer substrate, causing a significant amount of scattering. Several technical attempts, including chemical wet etching [12], oxidation, and smoothing [13] have produced improvement over the raw surface. In this paper, we present a novel technical approach with a manufacturable spin-coating process. The silicon surface coated with a thin layer of photoresist outperforms the surfaces treated by any other method in terms of roughness. A similar method to reduce the micromirror surface roughness was mentioned in [14], but without details. In this paper, atomic force microscopy (AFM) images are taken, and postmeasurement analysis with fast Fourier transform (FFT) is executed to quantitatively characterize the surface. Fig. 2(a) and (b) shows the AFM images of the silicon side wall after DRIE and the one that is spin coated with a 0.9-μm-thick AZ5209 photoresist. The root mean square is decreased from 6.9 to 0.44 nm.

The two-dimensional spatial power spectrum density (PSD), obtained by the FFT to the measured AFM data, clearly compares the effect of different surface treatments in Fig. 3. The other two samples are wet etched by 7 mol/l KOH solution in 75 °C for 30 s and 1050 °C wet oxidated for 4 h plus a 10 min buffered oxide etchant stripping. It is interesting to point out that in the low spatial frequency range ($< 0.1/\mu$m), the PSDs are approximately the same for all the four surfaces, which means the long-range fluctuation is not affected by the aforementioned surface treating methods. Scattering loss is primarily determined by high spatial frequency PSD, which is comparable to or shorter than the operating wavelength. In this range, the PSD of the spin-coated surface is at least one order of magnitude lower than the oxidation-smoothing method and two orders of magnitude lower than the wet etched or raw surfaces.

The master mold is composed of 12 parallel straight waveguides with 250 μm pitch and 50 $\times$ 50 $\mu\mathrm{m}^2$ cross-section. After the master mold is successfully prepared, a hard-molding fabrication process using ultraviolet (UV) embossing method is conducted on a 100-μm-thick topas film. The topas film is chosen

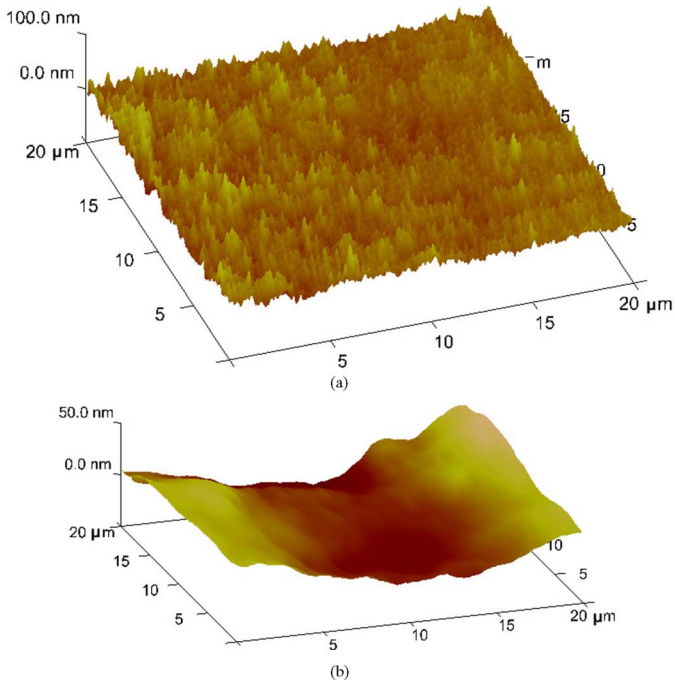

Fig. 2. AFM images of silicon surfaces (a) after DRIE and (b) after spin coating an AZ5209 photoresist layer.

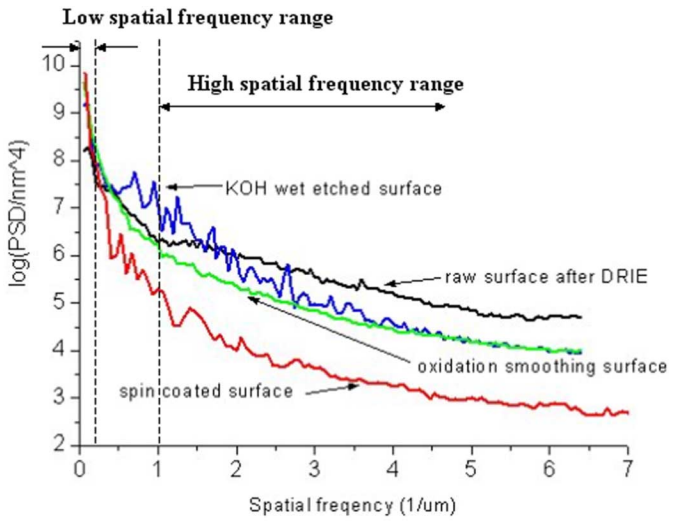

Fig. 3. PSD of silicon surfaces after different surface treatments.

because of its transparency and high glass transition temperature (Tg $>$ 160 °C) [10]. The main procedure is divided as the following steps shown in Fig. 4.

a) First, a layer of UV curable bottom cladding material [WIR30-450 (from ChemOptics), with a refractive index of 1.45 at 850 nm wavelength] is spin coated on the topas film substrate.
b) In the second step, the master mold is brought in contact with the spin-coated substrate, and the molded WIR30-450 layer is UV cured for 8 min inside a nitrogen atmosphere.
c) To separate the polymer substrate with the silicon master mold, the sample is immersed in acetone to quickly dissolve the photoresist layer on top of the silicon pattern. The intact polymer substrate will detach the master mold within 1 min. After forming the desired trenches, a core material WIR30-470 with a higher refractive index (1.47 at 850 nm) is used to fill them up. The excess polymer is scraped off, and the same amount of UV dose is applied to cure the core layer.
d) In the last step, the sample is spin coated with another layer of WIR30-450, which functions as the top cladding, and followed by a UV curing process.

Unlike hot embossing [15] or PDMS soft-molding [10] methods, there are no fabrication steps associated with high pressure or heating. This ensures the replicated waveguide array has an exact size as the original silicon master mold and thereby reduces the fabrication cost and energy consumption. The propagation loss of the waveguide is measured by the cutback method. An 850 nm VCSEL light is coupled into the waveguide by a 50/125 μm graded index multimode fiber and the output beam is then coupled into a photodetector by a 62.5/125 μm graded index multimode fiber. The measured propagation loss is 0.09 dB/cm at 850 nm. These data are close to the planar waveguide loss of 0.05 dB/cm provided by the material vendor. We also investigated the waveguide loss fabricated by other techniques, as listed in Table I. It clearly shows that the spin-coated surface treating method, plus the room temperature, zero pressure UV embossing process significantly reduces the waveguide loss.

IV. 45° Waveguide Micromirror

Waveguide couplers play a key role for the realization of three-dimensional fully embedded board-level optical interconnection owing to their surface-normal coupling of optical signals into and out of in-plane waveguides. A waveguide grating [9] as well as a 45° waveguide mirror-based coupler [11] can serve as a surface normal coupler. However, the grating-based approach requires precise control of grating parameters for efficient coupling and usually has a low tolerance to wavelength variations. Therefore, we employ 45° metal coated coupling mirrors at both ends of waveguides because they are easy to fabricate, reproducible, and relatively insensitive to wavelength variations and can provide a high coupling efficiency.

The coupling efficiency from the VCSEL to the waveguide can be simulated either by Gaussian beam method [10] or by ray-tracing method [16]. However, the real divergent angle of a VCSEL diode is usually much bigger than that of a Gaussian beam with the aperture-sized beam waist due to the existence of transverse multimodes. The nearly 100% calculated coupling efficiency from [10] is an ideal case. Ray-tracing method assumes the beam from VCSEL will travel in a straight line with 8–12° divergent angle, which is only true for far-field radiation. The distance from the VCSEL to the waveguide coupler is usually 50–500 μm in our architecture illustrated in Fig. 1. At this range, ray-tracing method will underrate the coupling efficiency. A more accurate simulation herein adopted is called M^2 factor revised Gaussian beam method [17], which semiempirically introduces a M^2 factor to define the beam quality. The M^2 factor defines the Gaussian beam to have the highest quality

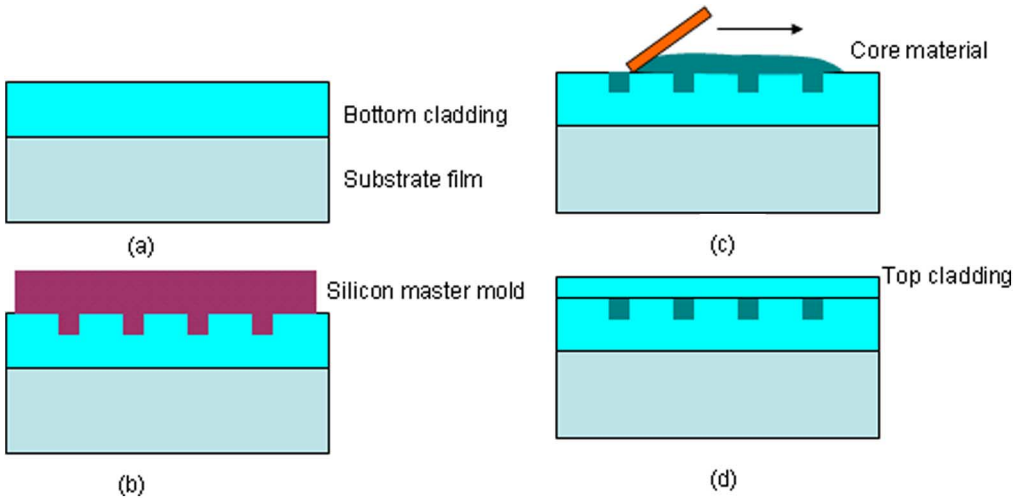

Fig. 4. UV embossed molding process of the polymer waveguide array.

TABLE I
PROPAGATION LOSS OF WAVEGUIDES FABRICATED BY DIFFERENT TECHNIQUES

Mold	Fabrication	Surface treating method	Waveguide(bottom cladding/core/top cladding)	Propagation loss (dB/cm)
Silicon	UV embossing	Spin-coated	WIR-450/WIR-470/WIR-450	0.09
Silicon	Hot embossing	Oxidation-smoothing	PMMA/WIR500/WIR470	0.26
Silicon	Hot embossing	Wet etched	PMMA/WIR500/WIR470	0.47
PDMS	Soft molding	N/A	WIR-450/WIR-470/WIR-450	0.16

with $M^2 = 1$ and multimode beams have a rating of $M^2 > 1$.[1] M is defined as

$$M = \left(\frac{w_{0M}}{w_0}\right) \tag{4.1}$$

where w_{0M} is the VCSEL aperture and w_0 stands for the equivalent Gaussian beam waist. The modified beam intensity can be expressed as

$$I(r,z) = \frac{2}{\pi w_{0M}^2(z)} \exp\left(\frac{-2r^2}{w_{0M}^2(z)}\right) \tag{4.2}$$

where

$$w_{0M}(z) = w_{0M}\left[1 + \left(\frac{M^2 z\lambda}{\pi w_{0M}^2}\right)^2\right]^{1/2}. \tag{4.3}$$

This definition implies that a VCSEL beam is larger than the corresponding single mode beam and diverges more rapidly. The VCSEL in this simulation has an optical aperture of 12 μm and a real half-beam divergent angle of 12°. Accordingly, the M factor calculated from (4.1) is 2.6. The distance from the VCSEL to the center of the 45° waveguide coupler is 50 μm (25 μm top cladding). With an index contrast of 0.02 between the core and cladding, the waveguide has an acceptance angle of 9.46°. Any incident light from the waveguide coupler that has a larger incident angle than 9.46° will eventually leaked from the waveguide. In the aforementioned model, the metal-coated mirror is assumed to have 100% reflectivity. Fig. 5(a) and (b) shows the coupling efficiency from the 12 μm aperture VCSEL to the 50 $\times$ 50 μm^2 waveguide through the micromirror as a function of the misalignment and mirror angular deviation, respectively. The maximum coupling efficiency is 90.5%. Unlike the simulation results from [10], the coupling efficiency is very sensitive to the angular deviation when Δn equals 0.01 and 0.02, because the divergent angle of the VCSEL diode is close to the waveguide acceptance angle. However, for strong index contrast waveguide ($\Delta n = 0.05$), which has a larger acceptance angle, the angular deviation tolerance can be as large as $\pm 4°$ for 70% coupling efficiency.

The waveguide micromirror can be fabricated by a one-step pattern transfer method described in [11]. After the DRIE process, the silicon master mold is mechanically polished on both ends using a specially designed 45° stage. The polishing process starts from a 30 μm grits lapping pad to 1 μm grits. Finer polishing is unnecessary since the following spin-coated

[1]Equations (4.1)–(4.3) are borrowed from [17].

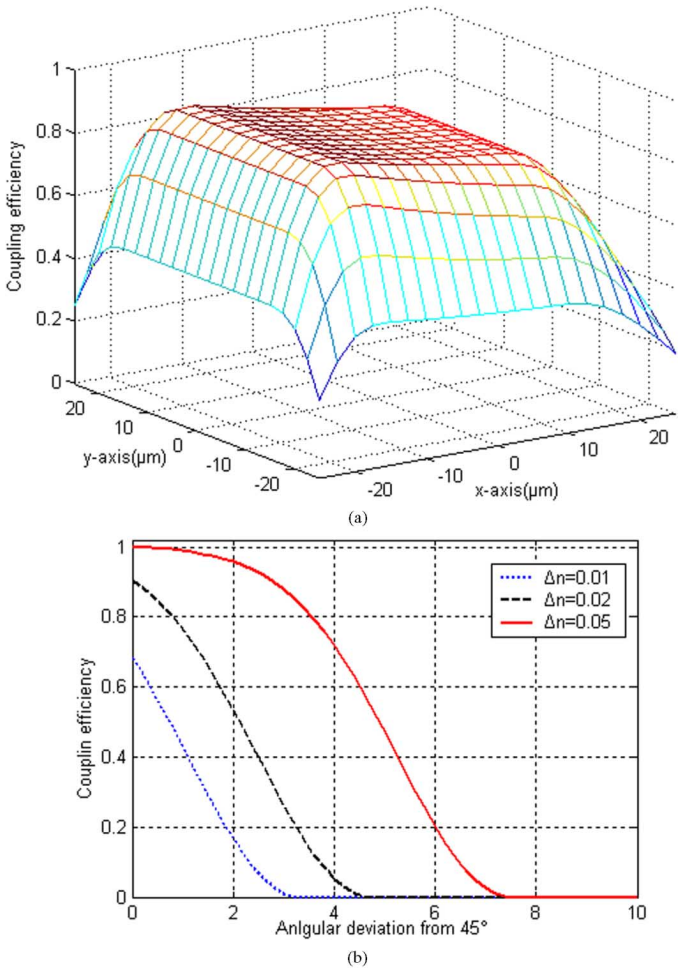

Fig. 5. Simulation coupling efficiency of the 45° micromirror as a function of (a) two-dimensional misalignment and (b) angular deviation of the micromirror.

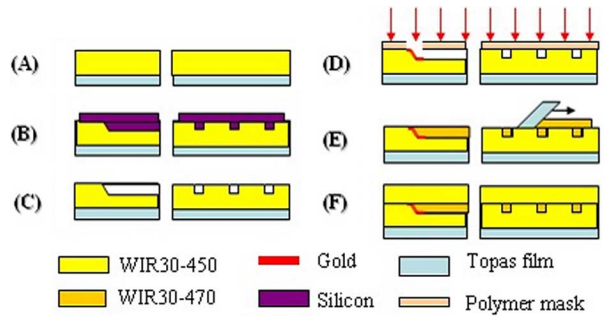

Fig. 6. Fabrication procedure of the polymer waveguide array with 45° waveguide micromirrors on both ends.

surface treating process will smear the remained roughness. The 45° tilted end surfaces will be transferred to the UV cross-linked polymer substrate that is in direct contact with the master mold. The waveguide array pattern, together with the desired micromirror coupler, is replicated in a negative shape from the master structure simultaneously. To further reduce the fabrication effort described in [11] using standard photolithography and followed by liftoff process, the sample is covered by a polymer thin-film mask with opened mirror

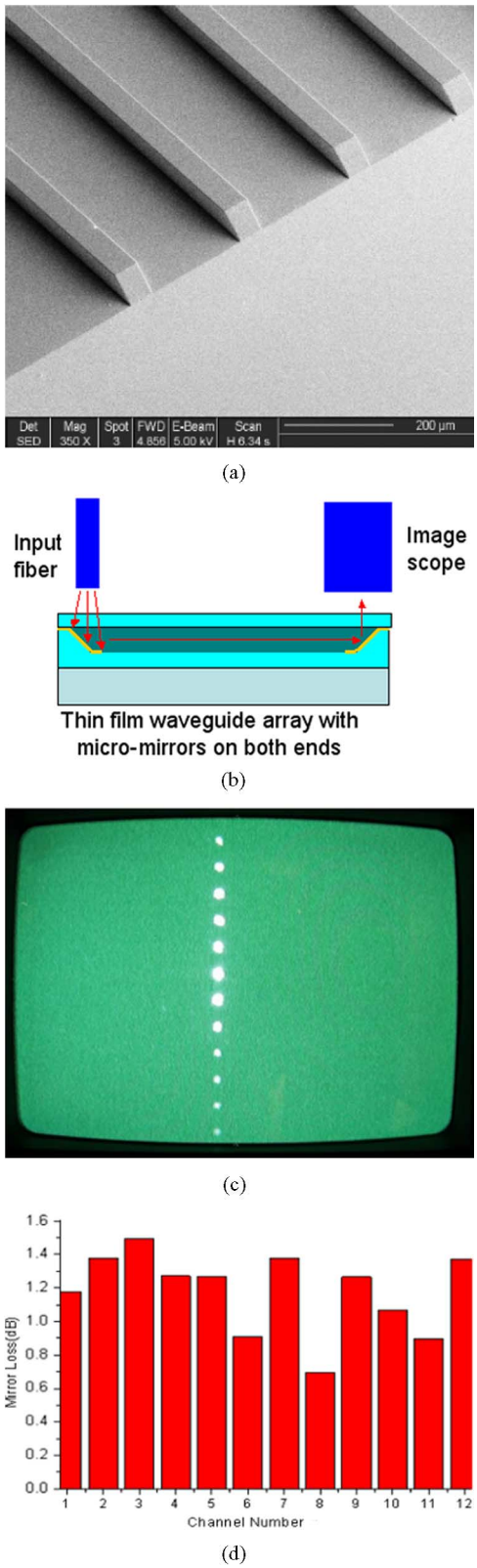

Fig. 7. Experimental results of the micromirror array. (a) SEM image of the silicon master mold with polished surface, (b) testing configuration, (c) output pattern from the image screen, and (d) measured coupling loss.

windows. This reusable thin-film mask will shield the deposition of metal layer on the polymer substrate except in the open windows. An electron beam evaporated 200 nm thick gold

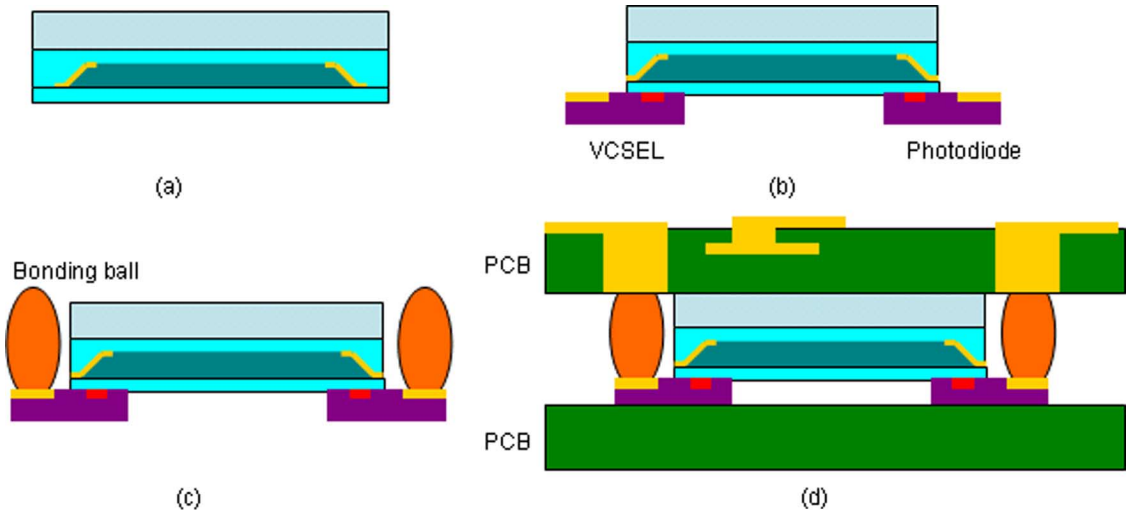

Fig. 8. Simplified integration procedure for fully embedded board-level optical interconnects.

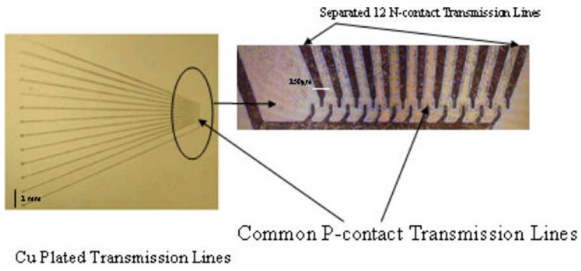

Fig. 9. Copper plated transmission lines on polymer substrate.

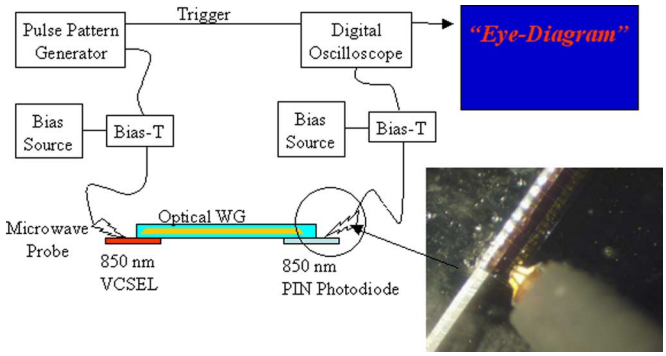

Fig. 10. Schematic diagram of the measurement setup for the assembled optical system.

layer is deposited to form the high reflectivity mirrors. After removing the thin-film mask, the UV embossed trenches with metal mirrors on both ends can be filled with the core material. The entire fabrication procedure is illustrated in Fig. 6. With this approach, a 51-cm-long polymer waveguide array has been successfully demonstrated, with a tested optical bandwidth of 150 GHz [18].

The scanning electron microscope (SEM) image of the polished surface on the silicon master mold is shown in Fig. 7(a). To observe the light transmission over the UV embossed waveguide array with the embedded 45° micromirrors, the sample tested with the configuration is shown in Fig. 7(b). A 9 μm core diameter fiber coupled with a 633 nm He-Ne laser vertically launches the input light into the waveguide mirrors. The input fiber is purposely pulled 5 mm above the mirror surface to coilluminate the 1×12 mirror array. At the back end, the output field patterns are projected onto an image scope, which can be viewed through a monitoring screen. The output patterns of the 12 reflecting mirrors are shown in Fig. 7(c). We measured the total insertion loss of the 12 channels at 850 nm wavelength. By comparing the results with the values for straight waveguides of the same length and dimension, we extracted the total coupling loss of the front and back mirrors. Assuming the two mirrors have the same coupling efficiency, which is approximately correct, the obtained coupling loss is 0.7–1.5 dB for each mirror, depicted in Fig. 7(d). In another word, the highest coupling efficiency is 85%.

V. Device Integration on Flexible Waveguide Film

The integration of active optoelectronic devices with the flexible waveguide film is the most important process among all the integration steps, including the final laminating process with the PCB. The proposed integration method through vias involves the following processes [10]: copper foil laminating, pattern alignment from back side, laser drilling through the topas film substrate, device bonding, and copper electroplating. To facilitate the fully embedded structure, we employ bonding ball to provide the vertical interconnects, which will implement the electrical-to-optical and optical-to-electrical conversions, as depicted in Fig. 8. The details of this via-free process are described in the following steps. Fig. 8(a) shows the thin-film waveguide array with embedded metal mirrors on both ends and Fig. 8(b) shows the polymer film, which is polished on both sides and terminates at 20 μm before the mirror position. This process can be precisely controlled by the polishing time and rate. Then, the VCSELs and photodiode array are bonded to the thin-film waveguide under a photoaligner. The alignment error can be controlled within ± 5 μm in both lateral and longitudinal directions. Fig. 8(c) illustrates flip-chip bonding balls, which are deposited on the bonding pads of the VCSELs and photodiode arrays. The total height of the optical layer is within 170 μm, which will fit the flip-chip bonding requirement. In the last step as Fig. 8(d)

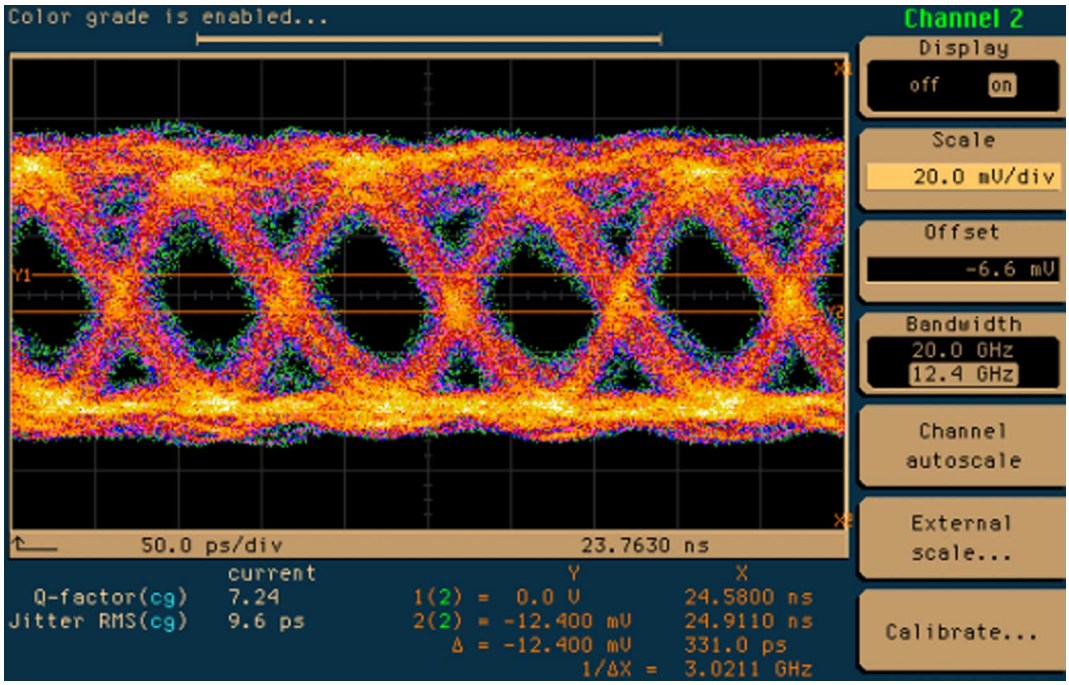

Fig. 11. Measured 10 Gbps eye diagram with a Q-factor of 7.24.

shows, the optical layer is laminated inside PCB layers with an easy alignment. Due to the small thickness of the optical layer with substrate removed VCSELs and photodiodes, and the reflow property of the polymer materials, the gap between the top and bottom PCBs will close and the PCB layers will be seamlessly laminated.

Some of the packaging efforts have been carried out and described in [10]. The design and fabrication of copper transmission lines and gold stud bumps were jointly developed with Sanmina SCI to facilitate the packaging processes described in [10], as shown in Fig. 9. The 12 N-transmission lines are arranged in an array and tapered in pitch from 2 mm to 250 μm to provide a high packaging density. The common P-transmission line almost reduced the line number by a factor of two. The transmission lines on the polymer film substrate will bridge the active optoelectronic components with on-board vias.

Fig. 10 shows the testing setup for the prototype optical layer with 8-cm-long waveguide array, which is embeddable to the PC boards (also suitable for surface mounted optical interconnects configuration), with an enlarged view of the microwave probes approached to the integrated photodiode array.

The VCSEL is biased with a lasing current, and the photocurrent from the p-i-n diode is measured as well. The maximum response from the photodiode is 300 μA when the VCSEL driving current reaches 12.5 mA. Considering the quantum efficiency of the VCSEL and responsivity of the photodiode, the emitting power from the VCSEL is calculated to be 2.9 mW, and the received power of the photodiode is 0.6 mW. The photocurrent from adjacent channels is measured to be less than 1 μA, indicating the optical crosstalk below 25 dB. The VCSEL is then biased at 5 mA and modulated by a $\pm$ 0.3 V 10 Gbps pseudorandom signal. The response from the photodiode is directly connected to a digital oscilloscope without any preamplification. The measured eye diagram is shown in Fig. 11, with a Q-factor of 7.24. If we assume the presence of Gaussian distributed noises, the relation between bit error rate (BER) and Q-factor can be expressed as[2]

$$\mathrm{BER} = \frac{1}{2} erfc\left(\frac{Q}{\sqrt{2}}\right). \tag{1}$$

The calculated BER is below 10^{-12}.

VI. Conclusion

This paper presented the latest progress of device fabrication and system integration for fully embedded board-level optical interconnects. A novel spin-coated surface treating method is used to smooth the silicon master mold and obtains a propagation loss of 0.09 dB/cm for the large cross-section waveguide, which is fabricated by a UV embossing molding process. The 45° micromirror is formed by a one-step pattern transfer from the master mold and is coated with a metal mirror by a photolithography-free process. The highest coupling efficiency of the micromirror is 85%. The system integration is simplified by a polish-and-bonding scheme, which requires less fabrication effort and reduces the cost. The optical signal transmission is implemented over the fully embeddable architecture with a 10 Gbps digital signal. The maximum photocurrent is measured to be 300 μA.

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