SECTION 4: MOSFETS

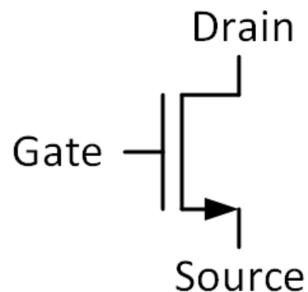
ECE 322 – Electronics I

MOSFET Device Introduction

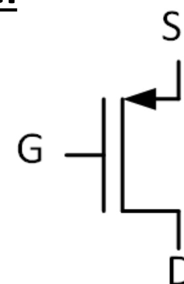
MOSFETs

- We now turn our attention to another type of transistor, the **MOSFET**:
  - **M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
- Many similarities to the BJT:
  - Three terminals
  - Voltage at one terminal controls current between the other two
    - A transconductance device
  - Two polarities: N-channel and P-channel MOSFETS
    - Our focus will primarily be N-channel MOSFETs (NMOS devices)

N-Channel (NMOS):



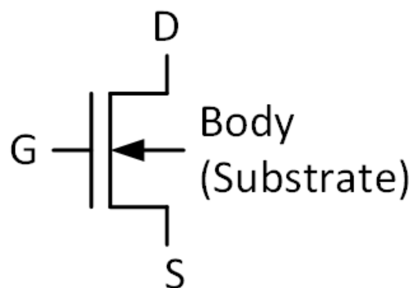
P-Channel (PMOS):



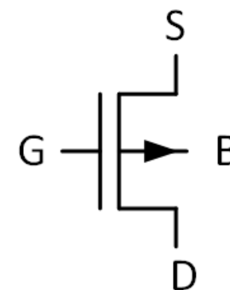
MOSFETs

- MOSFETs are actually ***four-terminal*** devices
  - Fourth terminal is the ***body***, ***substrate***, or ***bulk***
- The body is often tied to the source, and we can mostly ignore it
  - Discrete devices
- Other times we must account for the body potential effect on device behavior
  - Often the case in integrated circuits

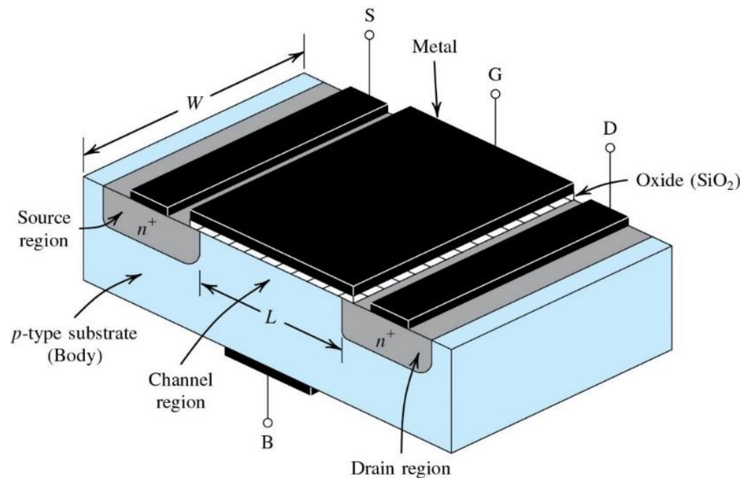
NMOS:

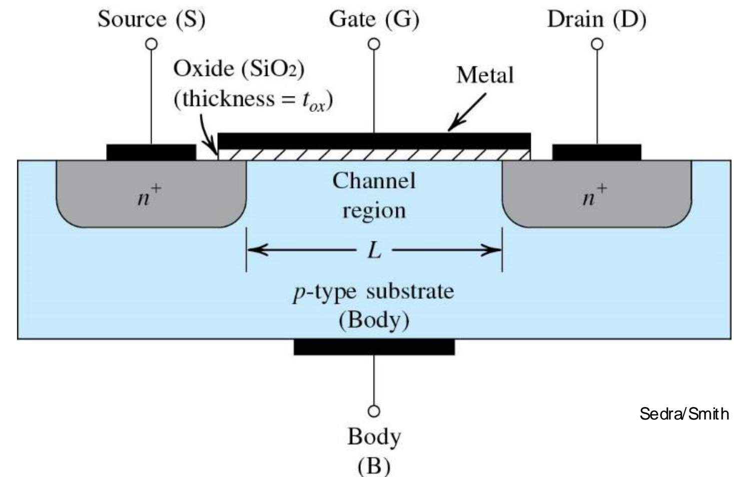


PMOS:



Physical Structure - NMOS





- P-type substrate
- N+ source and drain
- ***Metal gate electrode***, and source/drain/body contacts
- Thin ***oxide*** insulates the gate from the rest of the device
- Region of substrate between the drain and source is the ***channel***
  - Channel dimensions: W and L
  - We'll see later why this is called an n-channel (NMOS) device

Terminal Voltages and Currents

- Terminal voltages and currents named as shown
  - Again, lower-case v/i and upper-case subscript represents ***total*** (AC and DC) voltage and current
- For an NMOS device in typical operation:

$$v_{GS} \geq 0$$

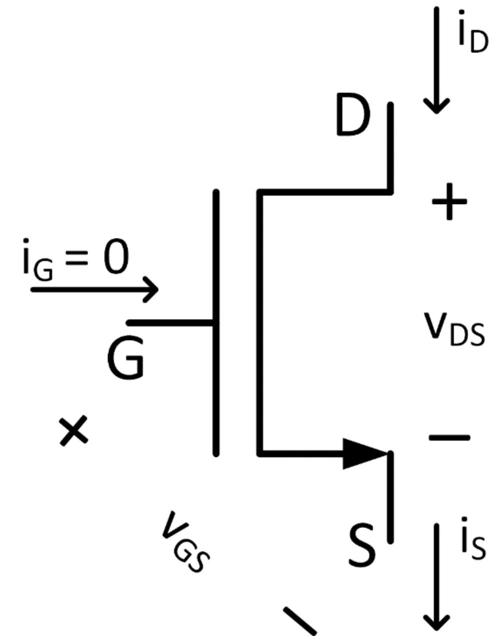
$$v_{DS} \geq 0$$

- Gate oxide does not allow current to flow, so

$$i_G = 0$$

and

$$i_D = i_S$$



MOSFET Operating Regions

- Three MOSFET operating regions:
  - Cut-off
  - Triode
  - Saturation

- A MOSFET's operating region is determined by its terminal voltages
- Next, we will look in detail at each of these three regions, along with their $i - v$ characteristics

Cut-Off Region

Cut-Off Region

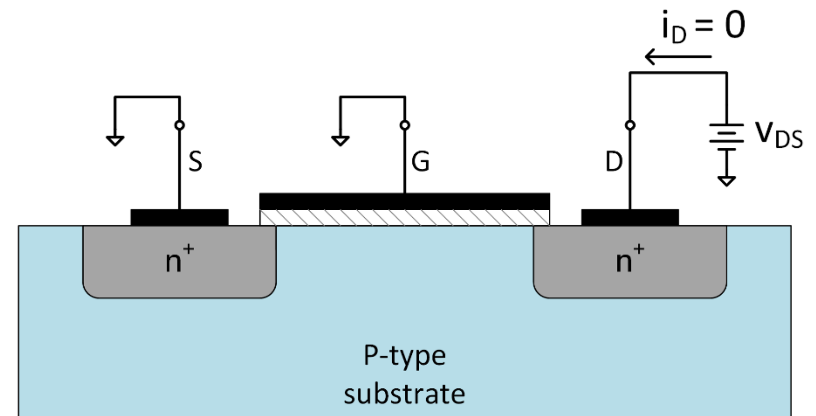
- Gate and source both grounded

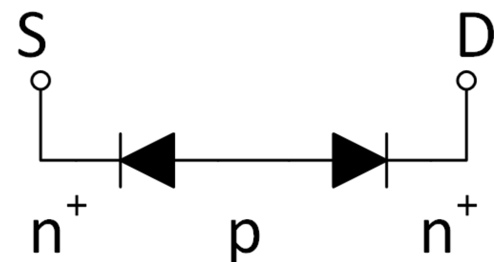
$$v_{GS} = 0$$

- Drain-to-source pathway looks like two back-to-back diodes
  - Very high drain-source resistance ($r_{DS} = \infty$)
- Even for $v_{DS} > 0$, no current will flow

$$i_D = 0$$

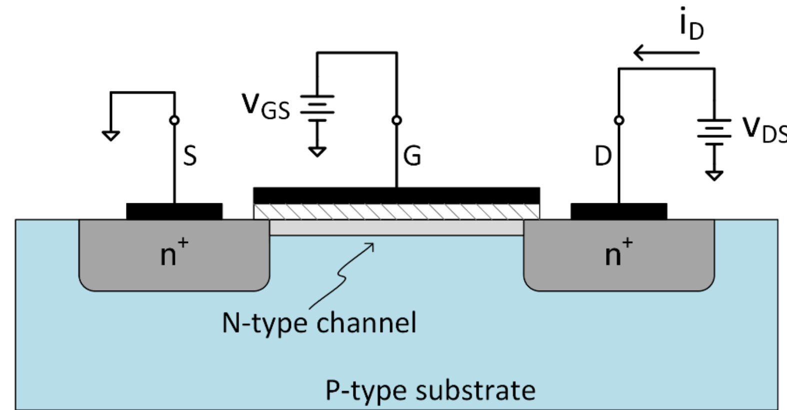
- Looks like an open switch
  - Similar to BJT cut-off operation





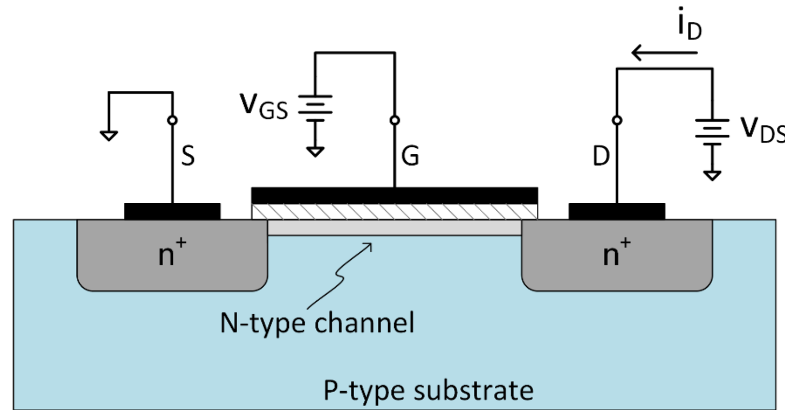
Triode Region

Triode Region – Inversion



- Now, v_{GS} is increased, while v_{DS} is kept small
  - Electric field established across gate oxide
  - Holes in p-type substrate repelled deeper into substrate
  - Electrons from drain and source attracted to region below the gate
- For large enough v_{GS}, p-type material below the gate is ***inverted*** to n-type
  - An ***inversion layer***
  - ***Induced n-type channel connects drain to source***
  - Now, current can flow in response to v_{DS}, $i_D > 0$

Threshold Voltage

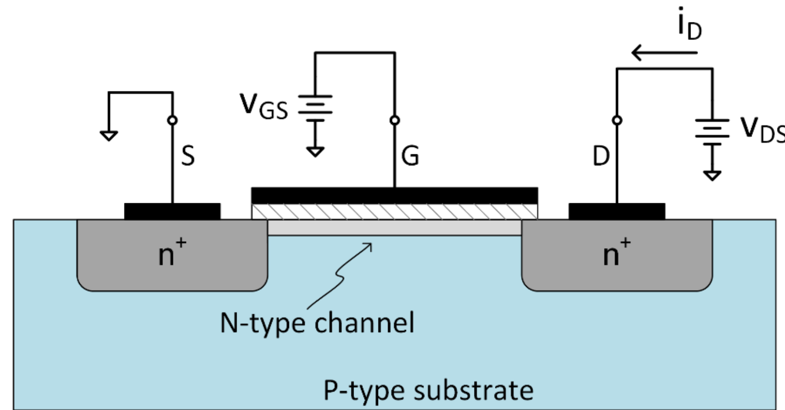


- Channel is induced once v_{GS} exceeds a certain voltage:
  - The ***threshold voltage***

$$v_{GS} \geq V_t$$

  - A device parameter
  - Typically, $V_t = 300\ mV \ldots 1\ V$
- As v_{GS} increases beyond V_t, the induced channel gets deeper
- As long as v_{DS} is small ($v_{DS} \ll V_t$), channel depth is uniform

Overdrive Voltage

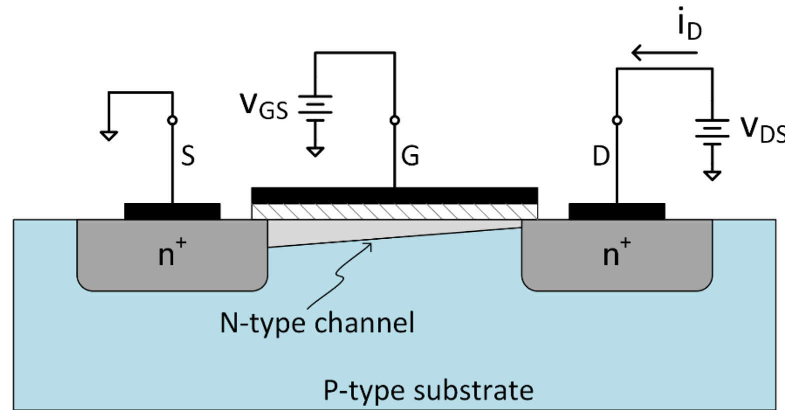


- A channel is induced once v_{GS} exceeds the threshold voltage
- v_{GS} in excess of the threshold voltage is called the ***overdrive voltage*** or ***effective voltage***:

$$v_{OV} = v_{GS} - V_t$$

- As we will soon see, v_{OV} plays an important role in determining device behavior

Triode Region



- As v_{DS} increases:
  - Voltage varies along the channel
    - v_S near the source, v_D near the drain
  - Gate-to-channel voltage decreases closer to the drain
  - Channel depth decreases closer to the drain
    - Channel is tapered
- More current flows with increasing v_{DS}, but channel resistance increases as channel becomes more tapered

Triode Region - i-v Relationship

- Drain current in the triode region:

$$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(v_{GS} - V_t) - \frac{1}{2}v_{DS}\right]v_{DS}$$

$$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[v_{OV} - \frac{1}{2}v_{DS}\right]v_{DS}$$

where:

- μ_n: electron mobility
- C_{ox}: oxide capacitance
- W: channel width
- L: channel length

- We can also express the drain current as

$$i_D = k_n'\left(\frac{W}{L}\right)\left[v_{OV} - \frac{1}{2}v_{DS}\right]v_{DS} = k_n'\left(\frac{W}{L}\right)\left[v_{OV}v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

where:

- $k_n' = \mu_n C_{ox}$ is the ***process transconductance parameter***

Triode Region - i-v Relationship

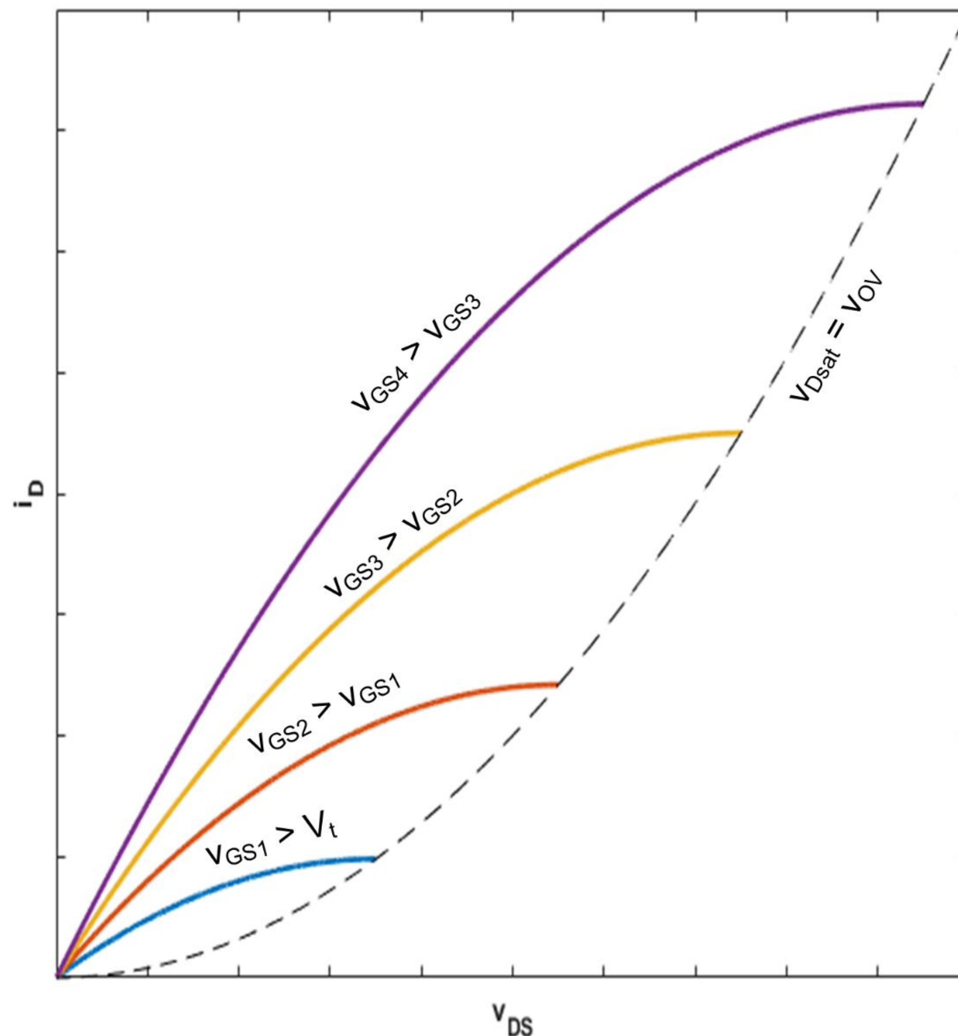
- Triode region:

$$v_{GS} > V_t$$
$$v_{DS} < v_{OV}$$

- For $v_{DS} \ll v_{ov}$
  - Nearly a linear resistance
  - Resistance linearly proportional to v_{OV}

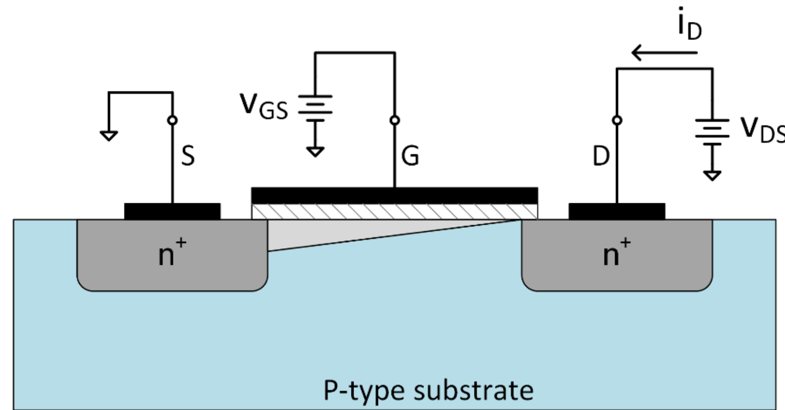
$$r_{DS} = \frac{1}{k_n' \frac{W}{L} v_{OV}}$$

- As v_{DS} increases
  - Channel taper increases
  - r_{DS} increases
  - i_D-v_{DS} slope decreases



Saturation Region

Device Operation – Channel Pinch-Off



- Eventually, for large enough v_{DS}
  - Gate-to-channel voltage near the drain no longer exceeds V_t
  - Channel ***pinch-off*** occurs
  - Channel disappears at the edge of the drain
- Pinch-off occurs when:

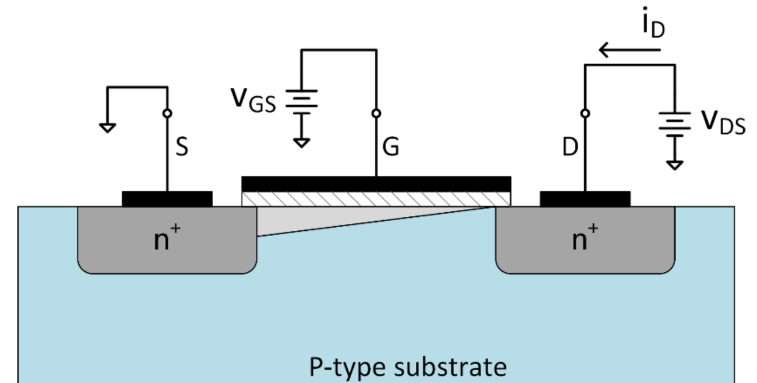
$$v_{GD} = V_t = v_{GS} - v_{DS}$$

$$v_{DS} = v_{GS} - V_t$$

$$\boxed{v_{DS} = v_{OV}}$$

Saturation Region

- Once channel pinch-off occurs:
  - Voltage at the drain-end of the channel remains v_{OV}, even as v_{DS} increases
  - Any increase in v_{DS} beyond v_{OV} is dropped across the depletion region surrounding the drain



  - Voltage across the length of the channel is fixed at v_{OV}
  - Pinched-off channel shape does not change with v_{DS}
  - Drain current ***saturates*** at a constant value for constant v_{GS}
  - Analogous to the forward-active region for BJTs

Saturation - i-v Relationship

- Drain current in the saturation region still given by

$$i_D = k_n' \left(\frac{W}{L}\right)\left[v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2\right]$$

- But now, the voltage from the drain-end to source-end of the channel is v_{OV}
- Replacing v_{DS} with v_{OV}, the drain current relationship becomes

$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) v_{OV}^2 = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (v_{GS} - V_t)^2$$

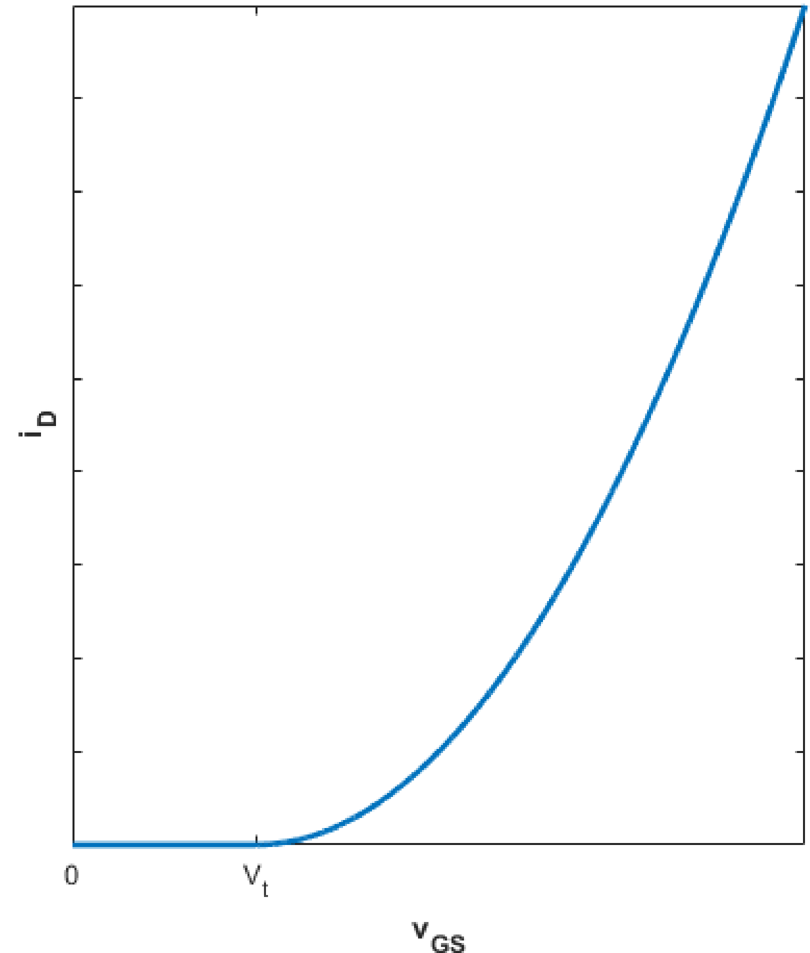
  - Purely a function of v_{GS} (or v_{OV})
  - Independent of v_{DS}

Input I-V Characteristic

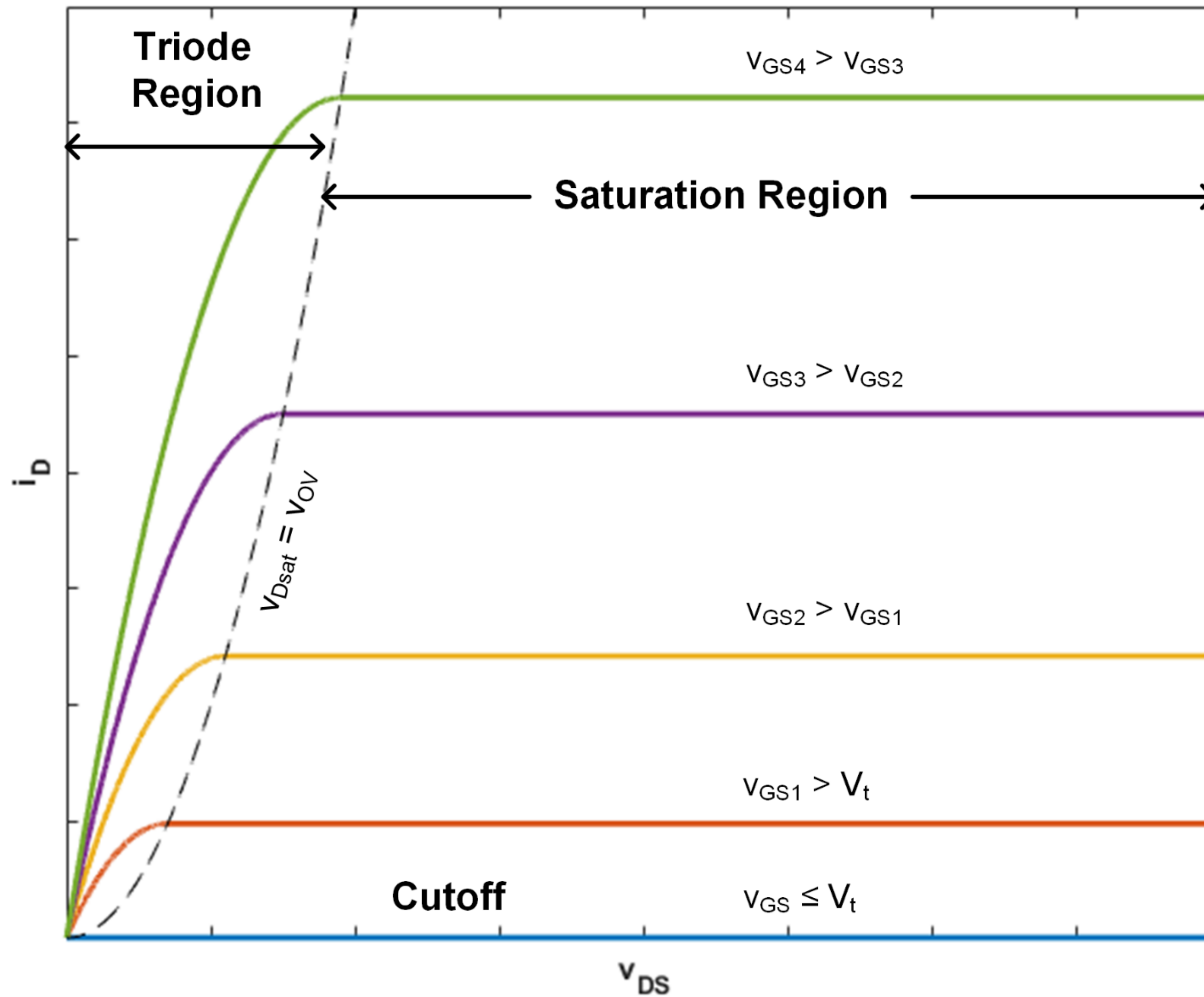
- In saturation, drain current has a ***quadratic*** dependence on v_{GS} (v_{OV})

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2$$

$$i_D = \frac{1}{2} k_n' \frac{W}{L} v_{OV}^2$$

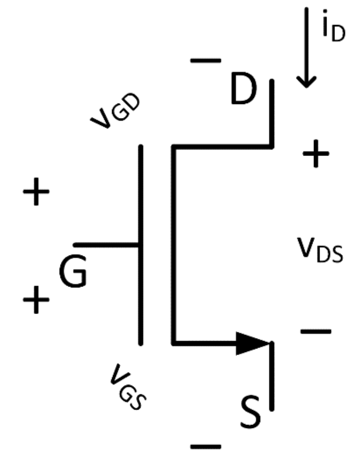


Output I-V Characteristic



NMOS Operating Regions – Summary

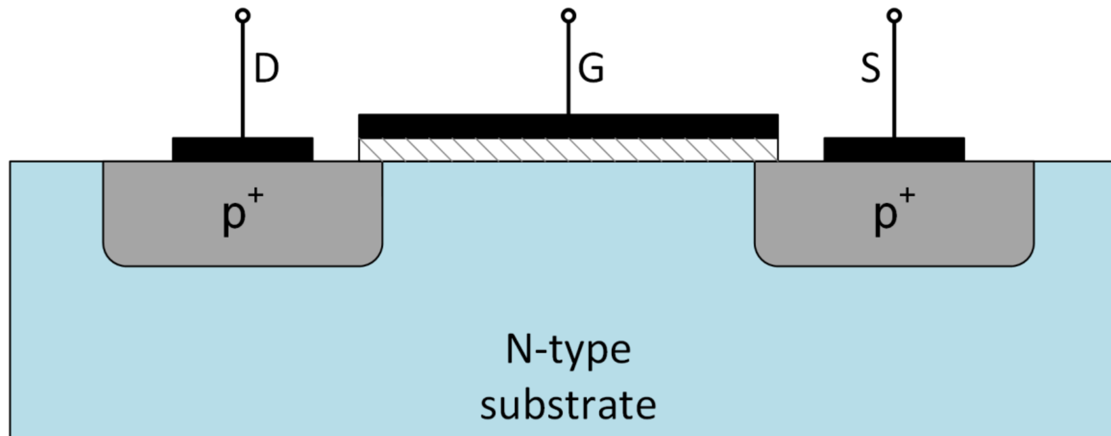
- **Cutoff**:
  - $v_{GS} < V_t$
  - $i_D = 0$
- **Triode**:
  - $v_{GS} > V_t$
  - $v_{DS} < v_{OV}$ or $v_{GD} > V_t$
  - $i_D = \mu_n C_{ox} \frac{W}{L} \left(v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2 \right) = k_n' \frac{W}{L} \left(v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2 \right)$
- **Saturation**:
  - $v_{GS} > V_t$
  - $v_{DS} > v_{OV}$ or $v_{GD} < V_t$
  - $i_D = \frac{1}{2} k_n' \frac{W}{L} \left(v_{GS} - V_{tp} \right)^2 = \frac{1}{2} k_n' \frac{W}{L} v_{OV}^2$



P-Channel MOSFETs

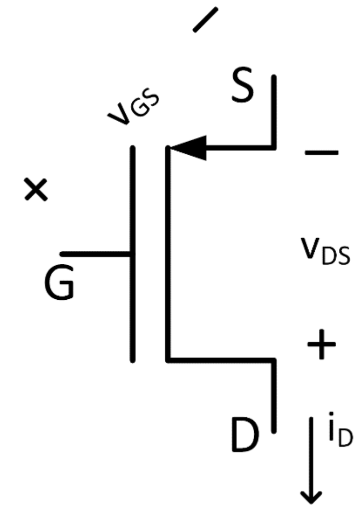
P-Channel MOSFETs

- Voltage polarities and doping types reversed relative to NMOS
  - N-type substrate
  - P^+ drain and source
  - Negative threshold voltage: $V_{tp} < 0$
  - Negative overdrive voltage: $v_{OV} = v_{GS} - V_{tp} < 0$
  - Channel induced for $v_{GS} \leq V_{tp}$
  - Substrate connected to source or most positive circuit voltage



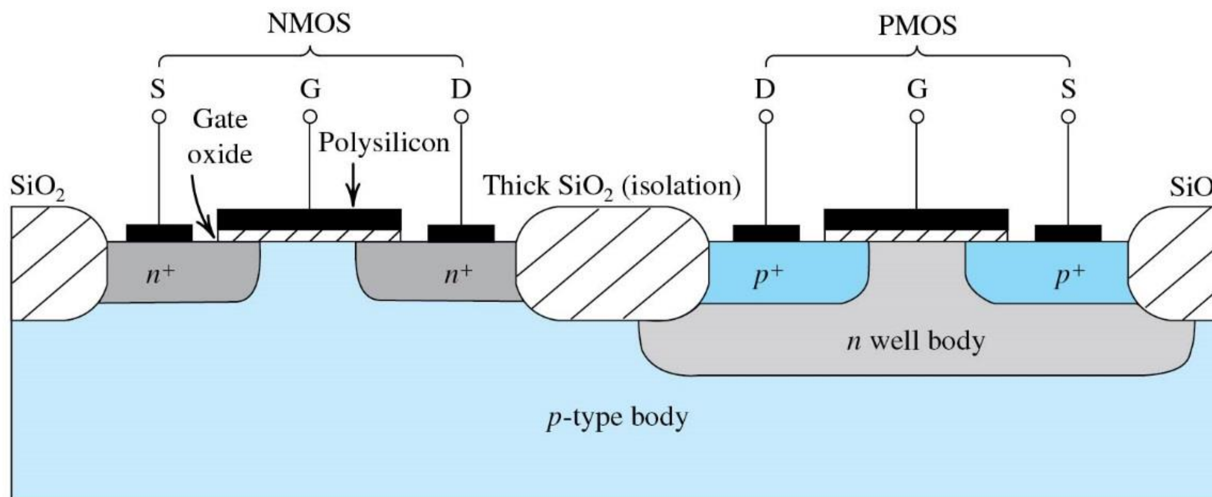
PMOS – Operating Regions

- **Cutoff**:
  - $v_{GS} > V_{tp}$
  - $i_D = 0$
- **Triode**:
  - $v_{GS} < V_{tp}, \quad |v_{GS}| > |V_{tp}|$
  - $v_{DS} > v_{OV}, \quad |v_{DS}| < |v_{OV}|$
  - $i_D = \mu_p C_{ox} \frac{W}{L} \left(v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2 \right) = k_p' \frac{W}{L} \left(v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2 \right)$
- **Saturation**:
  - $v_{GS} < V_{tp}, \quad |v_{GS}| > |V_{tp}|$
  - $v_{DS} < v_{OV}, \quad |v_{DS}| > |v_{OV}|$
  - $i_D = \frac{1}{2} k_p' \frac{W}{L} \left(v_{GS} - V_{tp} \right)^2 = \frac{1}{2} k_p' \frac{W}{L} v_{OV}^2$



CMOS

- Complementary MOS or ***CMOS***
  - Both NMOS and PMOS fabricated on the same chip
- P-type substrate
- PMOS devices fabricated in ***n wells***
- Most modern MOS chips are fabricated using CMOS technology



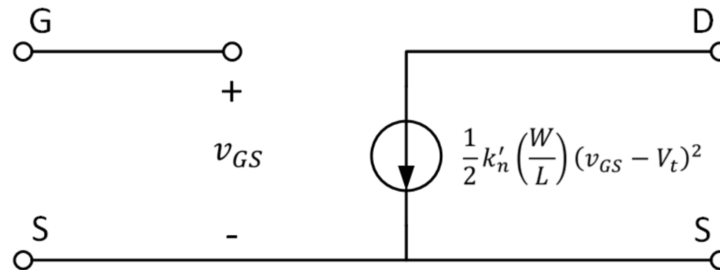
Large-Signal MOSFET Model

Equivalent Circuit Models

- As was the case for BJTs, we use two types of equivalent-circuit models for MOSFETs:
- ***Large-signal model***
  - Models the transistor's behavior to DC signals
  - Used to determine the transistor's DC operating point
- ***Small-signal model***
  - Models the behavior in response to small signals
  - Describes the response to the AC signals to be amplified
  - Properties of the small-signal model determined by the DC operating point

Large-Signal Model – Saturation

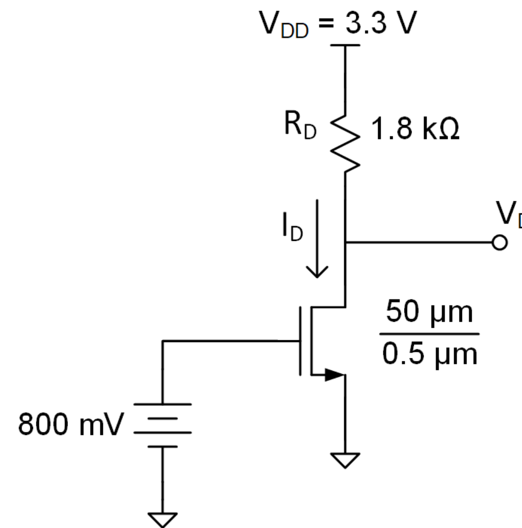
- Large-signal behavior in the saturation region is modeled by the following circuit:



- Replace the transistor with the appropriate model to determine the DC operating point (Q-point)
- Saturation-region bias assumed
  - If incorrect, model will say otherwise
- Because $i_G = 0$, ***we generally do not need to explicitly use the equivalent circuit model for large-signal analysis for MOSFETs***
  - Often just use the I-V model

DC Operating Point – Example 1

- Determine I_D and V_D for the following circuit
  - Is the device operating in the saturation region?



$\mu_n = 500 \frac{cm^2}{V \cdot s}$

$C_{ox} = 3.8 \frac{fF}{\mu m^2}$

$V_t = 500\ mV$

$L = 0.5\ \mu m$

$W = 50\ \mu m$

- The process transconductance parameter:

$$k_n' = \mu_n C_{ox} = 500 \times 10^{-4} \frac{m^2}{V \cdot s} \cdot \frac{3.8 \times 10^{-15}\ F}{1 \times 10^{-12}\ m^2} = 190 \frac{\mu A}{V^2}$$

- Use the saturation region large-signal model
  - I-V model, not necessarily the equivalent-circuit model
  - Analysis will indicate if saturation assumption is incorrect

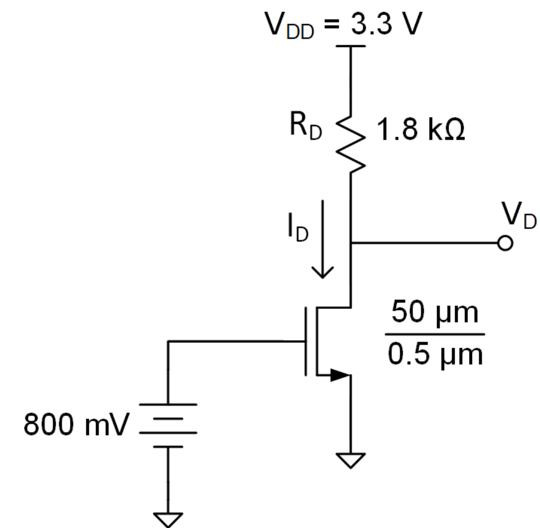
DC Operating Point – Example 1

- Drain current in saturation:

$$I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (V_{GS} - V_t)^2$$

$$I_D = \frac{1}{2} \cdot 190 \frac{\mu A}{V^2} \cdot \left(\frac{50\ \mu m}{0.5\ \mu m}\right) (800\ mV - 500\ mV)^2$$

$$\boxed{I_D = 855\ \mu A}$$



- Voltage at the drain:

$$V_D = V_{DD} - I_D R_D$$

$$V_D = 3.3\ V - 855\ \mu A \cdot 1.8\ k\Omega$$

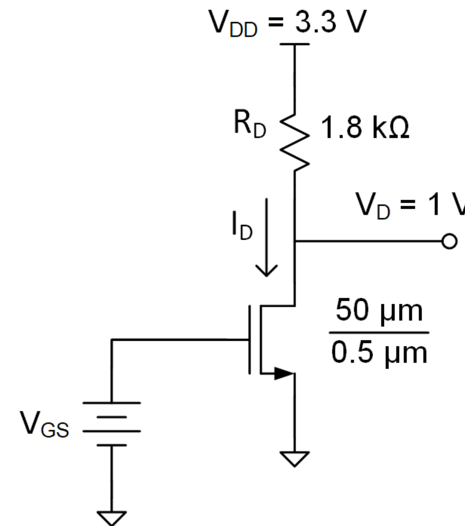
$$\boxed{V_D = 1.76\ V}$$

- The device is operating in the saturation region
  - The drain-to-source voltage exceeds the overdrive voltage

$$V_{DS} = V_D = 1.76\ V > V_{OV} = V_{GS} - V_t = 300\ mV$$

DC Operating Point – Example 2

- For the same circuit, determine V_{GS} for $V_D = 1\ V$
  - Is the device still operating in the saturation region?



$$\mu_n = 500\frac{cm^2}{V \cdot s}$$

$$C_{ox} = 3.8\frac{fF}{\mu m^2}$$

$$V_t = 500\ mV$$

$$L = 0.5\ \mu m$$

$$W = 50\ \mu m$$

- For $V_D = 1\ V$

$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{3.3\ V - 1\ V}{1.8\ k\Omega}$$

$$I_D = \frac{2.3\ V}{1.8\ k\Omega} = 1.28\ mA$$

- Assuming saturation-region operation

$$I_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)V_{OV}^2 = \frac{1}{2} \cdot 190\frac{\mu A}{V^2} \cdot \left(\frac{50\ \mu m}{0.5\ \mu m}\right) \cdot V_{OV}^2 = 1.28\ mA$$

- Solving for the overdrive voltage

$$V_{OV} = 367\ mV$$

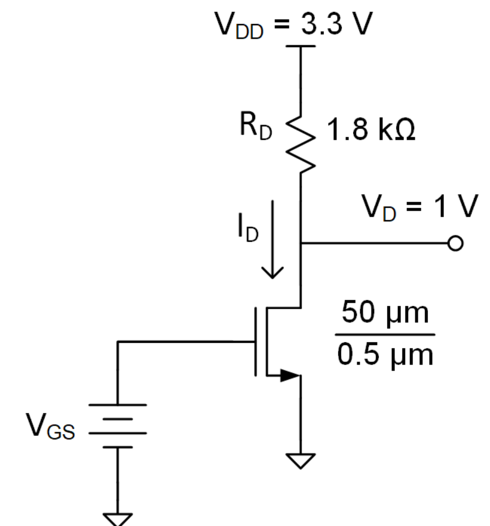
DC Operating Point – Example 2

- The required gate-to-source voltage is

$$V_{GS} = V_t + V_{OV}$$

$$V_{GS} = 500\ mV + 367\ mV$$

$$\boxed{V_{GS} = 867\ mV}$$



- The drain-to-source voltage exceeds the overdrive voltage
  - The transistor is operating in the saturation region

$$V_{DS} = 1V > V_{OV} = 367\ mV$$

DC Operating Point – Example 3

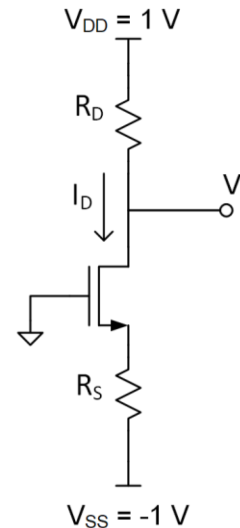
- Find R_D and R_S for

$$I_D = 200\ \mu A \text{ and } V_D = 200\ mV$$

- First, determine R_D

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{1\ V - 200\ mV}{200\ \mu A}$$

$$\boxed{R_D = 4\ k\Omega}$$



$$k_n' = 400\ \frac{\mu A}{V^2}$$

$$V_t = 500\ mV$$

$$L = 0.5\ \mu m$$

$$W = 15\ \mu m$$

- Drain current in saturation is given by

$$I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) V_{OV}^2 \rightarrow V_{OV} = \sqrt{\frac{2 I_D}{k_n'} \frac{L}{W}}$$

$$V_{OV} = \sqrt{\frac{2 \cdot 200\ \mu A}{400\ \mu A/V^2} \frac{0.5 \mu m}{15\ \mu m}} = 182.6\ mV$$

DC Operating Point – Example 3

- The gate-to-source voltage is

$$V_{GS} = V_t + V_{OV} = 500\ mV + 182.6\ mV$$

$$V_{GS} = 683\ mV$$

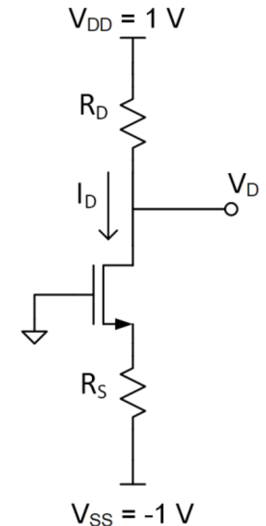
- The gate is grounded, so the source voltage is

$$V_S = V_G - V_{GS} = -683\ mV$$

- The source resistance is given by

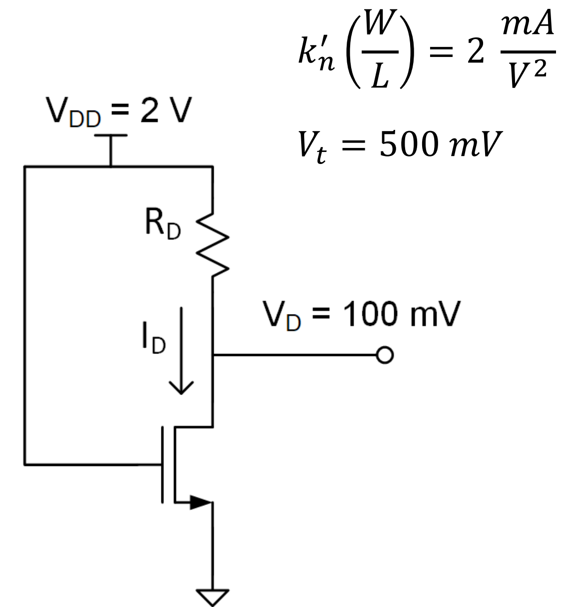
$$R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-683\ mV - (-1\ V)}{200\ \mu A}$$

$$\boxed{R_S = 1.59\ k\Omega}$$



DC Operating Point – Example 4

- Find I_D and R_D for $V_D = 100\ mV$
  - What is the drain-to-source resistance, r_{DS}?



- The device is in the triode region:

$$V_{OV} = V_{GS} - V_t = 2\ V - 500\ mV = 1.5\ V$$

$$V_{DS} = 100\ mV < V_{OV}$$

- Drain current in triode is given by

$$I_D = k_n'\left(\frac{W}{L}\right)\left(V_{OV} - \frac{1}{2}V_{DS}\right)V_{DS}$$

$$I_D = 2\frac{mA}{V^2}(1.5\ V - 50\ mV)100\ mV$$

$$\boxed{I_D = 290\ \mu A}$$

DC Operating Point – Example 4

- The required drain resistance:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{1.9\ V}{290\ \mu A}$$

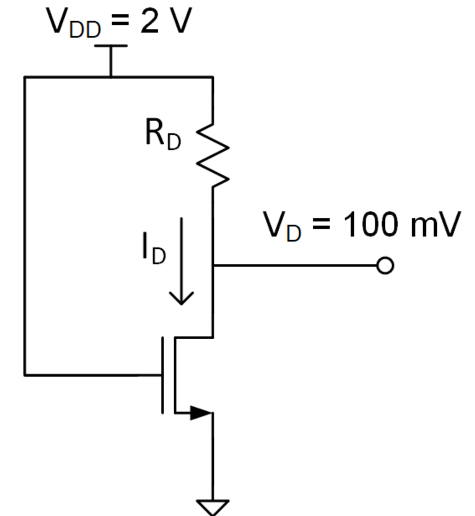
$$\boxed{R_D = 6.55\ k\Omega}$$

- The drain-to-source resistance in the triode region is given by:

$$r_{DS} = \frac{1}{k_n' \frac{W}{L} V_{OV}}$$

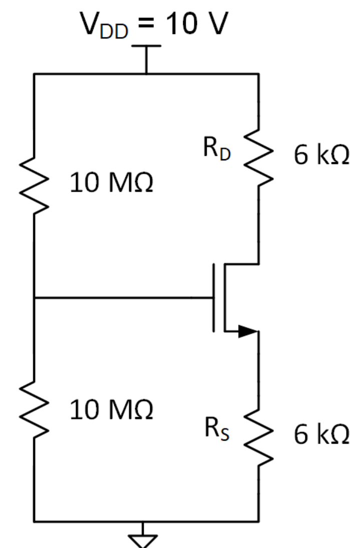
$$r_{DS} = \frac{1}{2 \frac{mA}{V^2} 1.5\ V}$$

$$\boxed{r_{DS} = 333\ \Omega}$$



DC Operating Point – Example 5

- Find I_D, V_G, V_D, and V_S for the following circuit



$$k_n'\left(\frac{W}{L}\right) = 1\,\frac{mA}{V^2}$$

$$V_t = 1\,V$$

- The gate voltage is simply set by the voltage divider

$$V_G = 10\,V\,\frac{10\,M\Omega}{10\,M\Omega + 10\,M\Omega}$$

$$\boxed{V_G = 5\,V}$$

- Assuming operation in the saturation region, drain current is

$$I_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)^2 = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(V_G - I_D R_S - V_t)^2$$

$$I_D = 0.5\,\frac{mA}{V^2}(5\,V - I_D R_S - 1\,V)^2$$

DC Operating Point – Example 5

$$I_D = 0.5\frac{mA}{V^2}(4\,V - I_D \cdot 6\,k\Omega)^2$$

- This is a quadratic equation for I_D

$$I_D = 18E3\,I_D^2 - 24\,I_D + 8E - 3$$

- Two possible solutions:

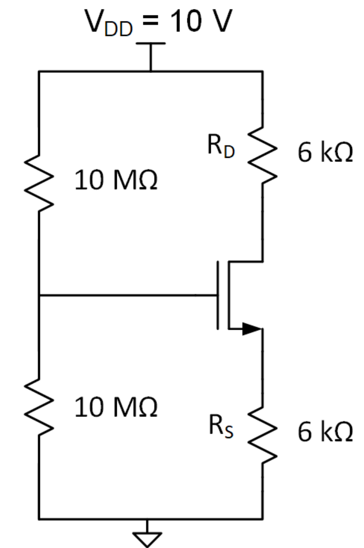
$$I_D = 889\,\mu A \text{ or } I_D = 500\,\mu A$$

- For $I_D = 889\,\mu A$

$$V_D = V_{DD} - I_D R_D = 10\,V - 889\,\mu A \cdot 6\,k\Omega = 4.67\,V$$

$$V_S = I_D \cdot R_S = 889\,\mu A \cdot 6\,k\Omega = 5.33\,V$$

$$V_{GS} = V_G - V_S = -333\,mV$$



DC Operating Point – Example 5

- For $I_D = 889\ \mu A$
  - $V_{GS} < 0$
  - The transistor is in the cut-off region
- The valid solution to the quadratic equation must be

$$I_D = 500\ \mu A$$

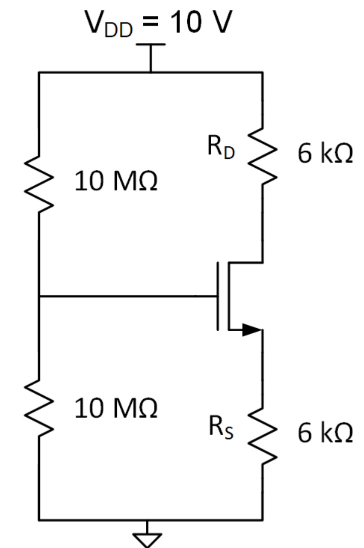
- The drain and source voltages are

$$V_D = V_{DD} - I_D R_D = 10\ V - 500\ \mu A \cdot 6\ k\Omega$$

$$V_D = 7\ V$$

$$V_S = I_D \cdot R_S = 500\ \mu A \cdot 6\ k\Omega$$

$$V_S = 3\ V$$



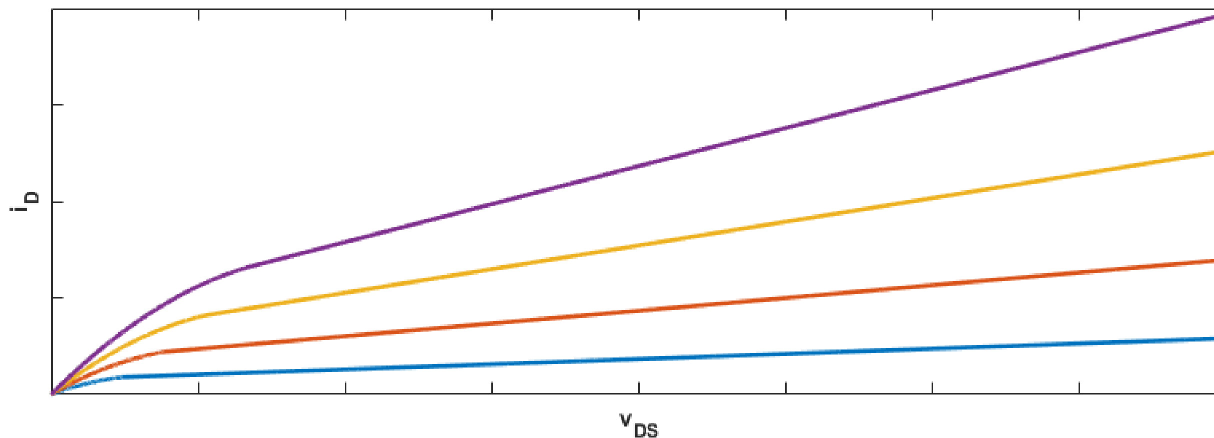
Channel-Length Modulation

Channel-Length Modulation

- So far, our MOSFET model in the saturation region models drain current as independent of v_{DS}

$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) v_{OV}^2$$

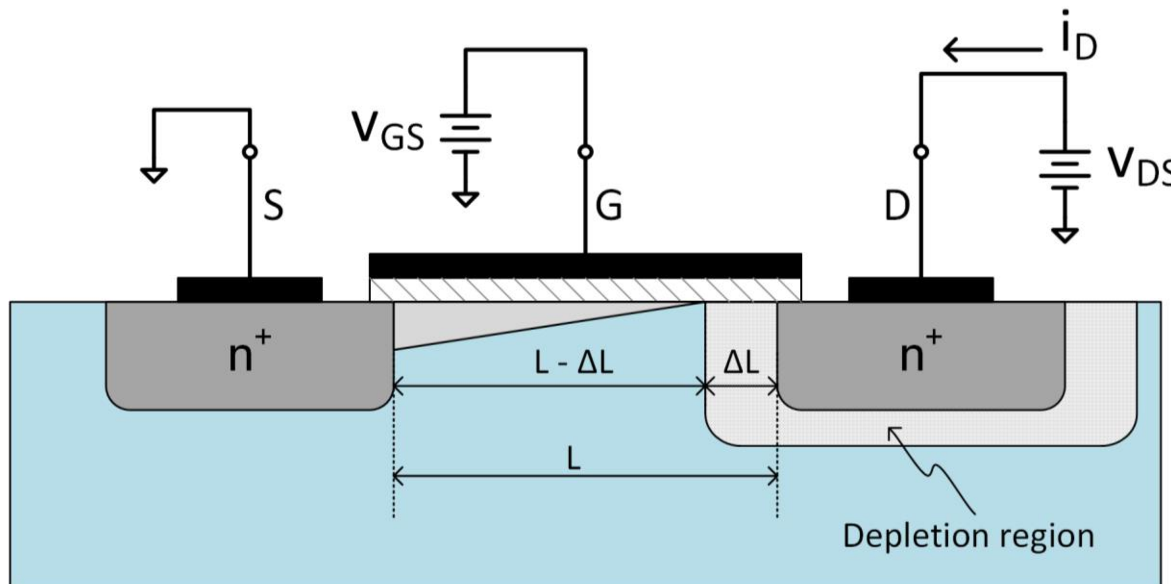
  - Flat I-V characteristic in the saturation region
- In reality, current increases as v_{DS} increases



- Increase in i_D due to ***channel-length modulation***

Channel-Length Modulation

- Justification for constant saturation current was:
  - Channel shape does not change after pinch-off occurs
  - Any additional v_{DS} is dropped across the depletion region surrounding the drain
- ***But, as v_{DS} increases, the drain depletion region increases, and the channel length decreases***

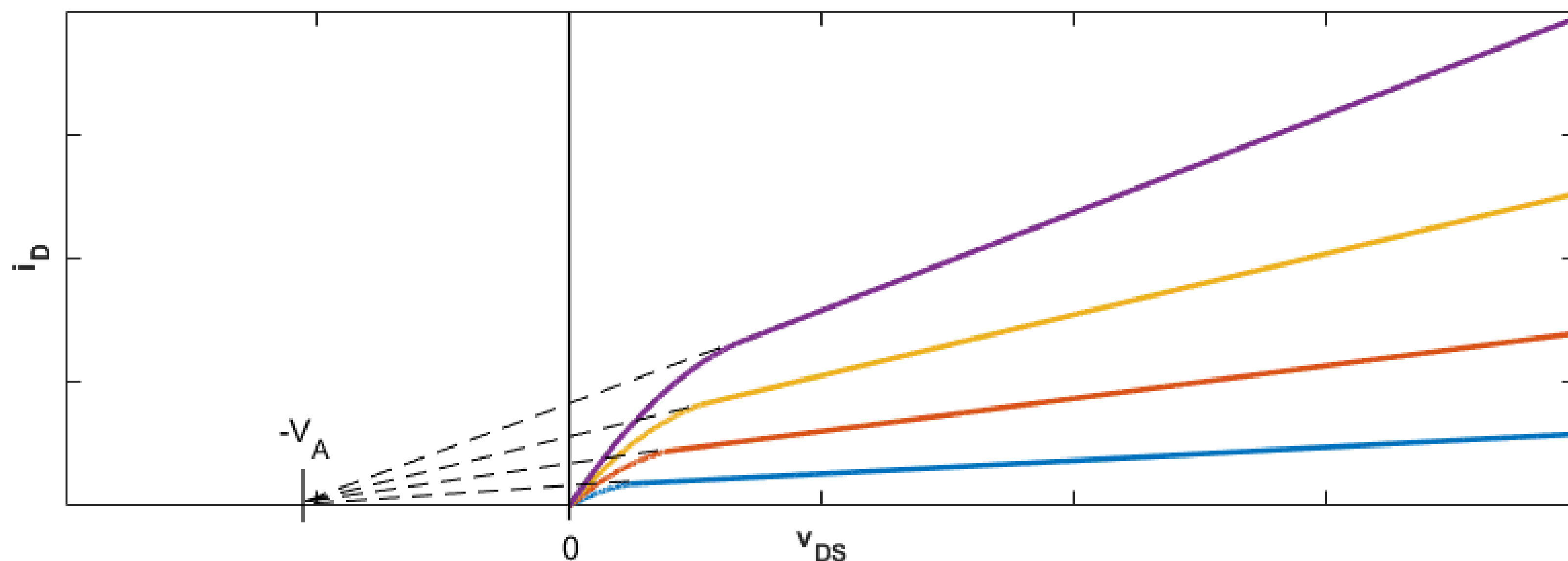


Channel-Length Modulation

- Drain current is inversely proportional to channel length

$$i_D \propto \frac{1}{L}$$

- So, as v_{DS} increases, L decreases, and i_D increases
  - Non-zero slope in the saturation region of the i_D-v_{DS} curve:

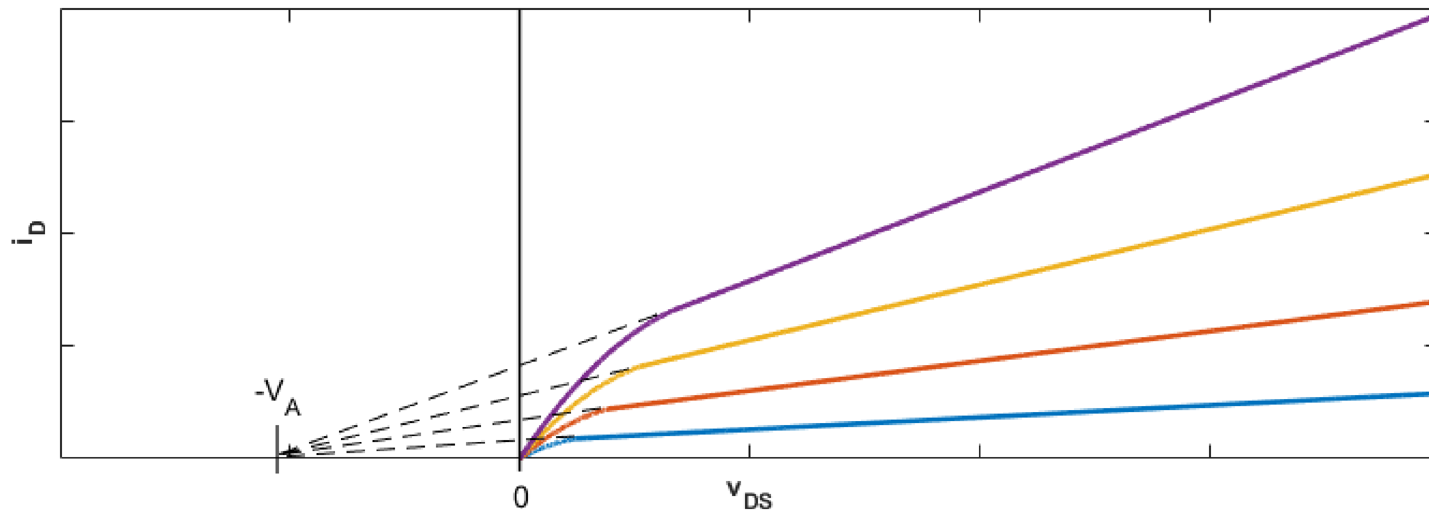


Channel-Length Modulation

- This effect is accounted for by the ***channel-length modulation parameter***, λ

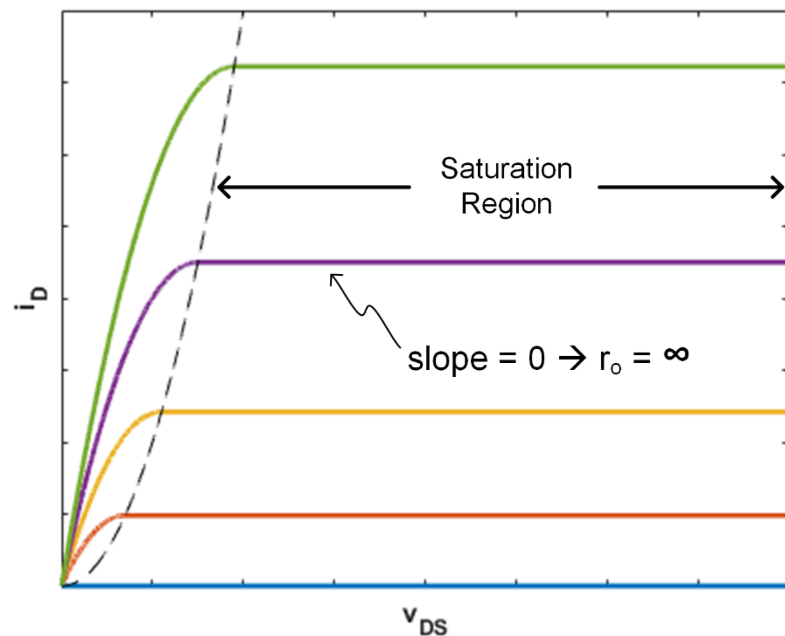
$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2 (1 + \lambda v_{DS})$$

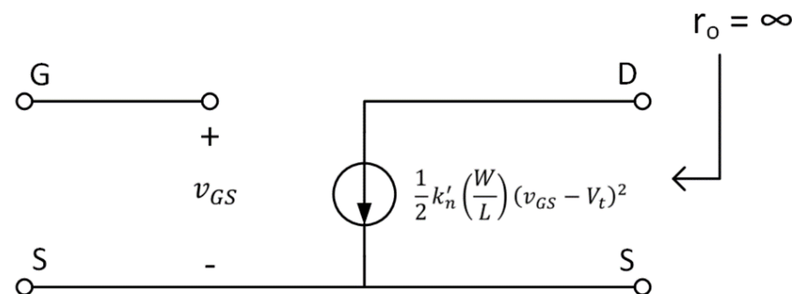
  - λ is inversely proportional to channel length, L
  - λ related to the ***Early voltage***: $\lambda = \frac{1}{V_A}$



Output Resistance

- Slope of the i_D-v_{DS} characteristic is the inverse of the transistor's ***output resistance***
  - Resistance seen looking into the drain
- Constant saturation current implies ***infinite output resistance***



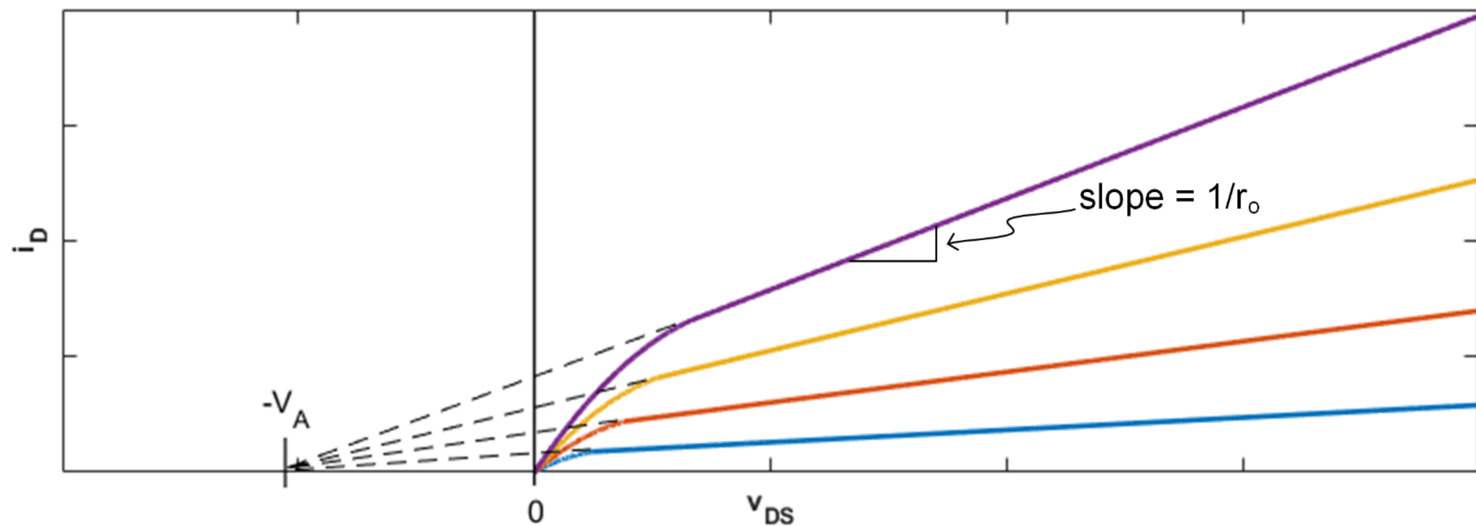


Output Resistance

- Output resistance given by

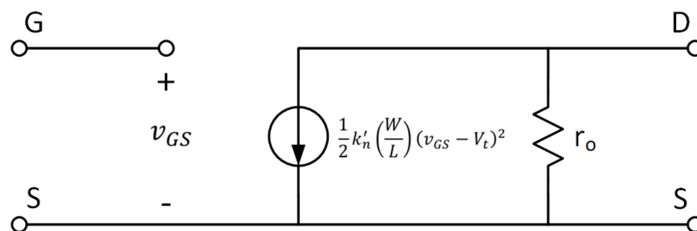
$$r_o = \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}$$

  - The inverse of the slope of the i_D-v_{DS} characteristic
- Channel-length modulation results in finite output resistance



Output Resistance

- Model the finite output resistance due to channel-length modulation by adding a resistor to our large-signal model



- Output resistance given by

$$r_o = \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1} = \left[\frac{\partial}{\partial v_{DS}}\left(\frac{1}{2}k_n'\frac{W}{L}(v_{GS}-V_t)^2(1+\lambda v_{DS})\right)\right]^{-1}$$

$$r_o = \left[\frac{\lambda}{2}k_n'\frac{W}{L}(v_{GS}-V_t)^2\right]^{-1}$$

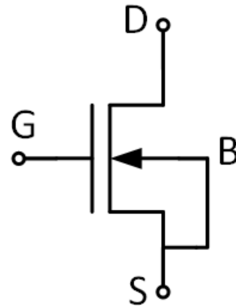
$$r_o = \frac{1}{\lambda I_D'} = \frac{V_A}{I_D'}$$

The Body Effect

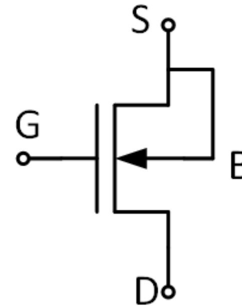
The Body Effect

- So far, we have largely ignored the connection to the substrate
  - Equivalently, we have assumed it to be tied to the source:

NMOS:



PMOS:



- This a valid assumption for ***discrete*** devices
  - Not so for MOSFETs on integrated circuits (ICs)

The Body Effect

- For integrated circuits, the substrate is typically tied to the most negative supply voltage for NMOS devices
  - PMOS n-wells tied to the most positive supply voltage
- Substrate for a given device may well be biased below its source voltage (above for PMOS)
  - This is the bias voltage for the channel region
- ***For*** $V_{SB} > 0$ ($V_{SB} < 0$ for PMOS), the ***threshold voltage is effectively increased***
  - This is the ***body effect***

MOSFETs as Switches

MOSFETs as Switches

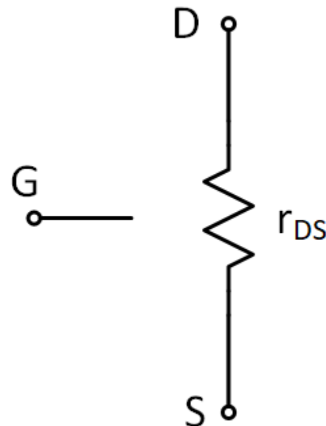
- Our focus is on the use of MOSFETs for ***linear amplifiers*** in ***analog circuits***
  - Operation in the ***saturation*** region
- MOSFETs are also useful as ***switches*** in ***digital circuits***
  - Microprocessors contain *billions* of MOSFETs used as switches on a single chip
- When operating as a switch, MOSFETs alternate between the ***triode*** (on, closed) and ***cutoff*** (off, open) regions

Triode/Cutoff Region Models

- MOSFETs used as ***switches*** operate alternately in the ***triode*** (closed) and ***cutoff*** (open) regions
- Equivalent circuit models:

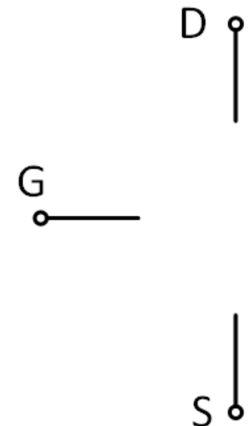
Triode Region (ON):

- $V_{GS} > V_t$
  - $V_{GS} = V_{DD}$
- Switch is on
- $I_D \geq 0$
- $V_{DS} = I_D r_{DS} < V_{OV}$



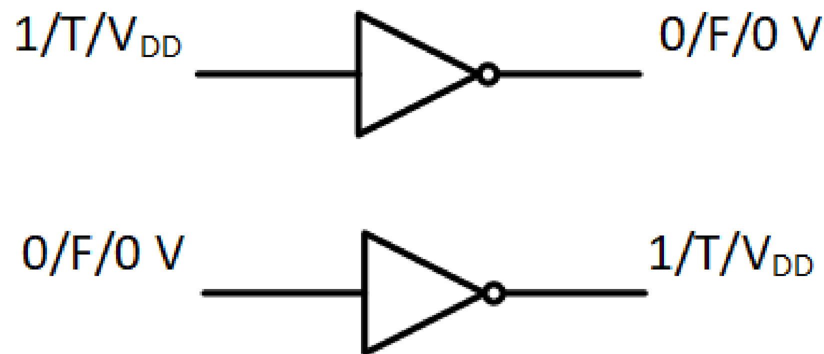
Cutoff Region (OFF):

- $V_{GS} < V_t$
  - $V_{GS} = 0$
- Switch is off
- $I_D = 0$
- $V_{DS} = V_{DD}$



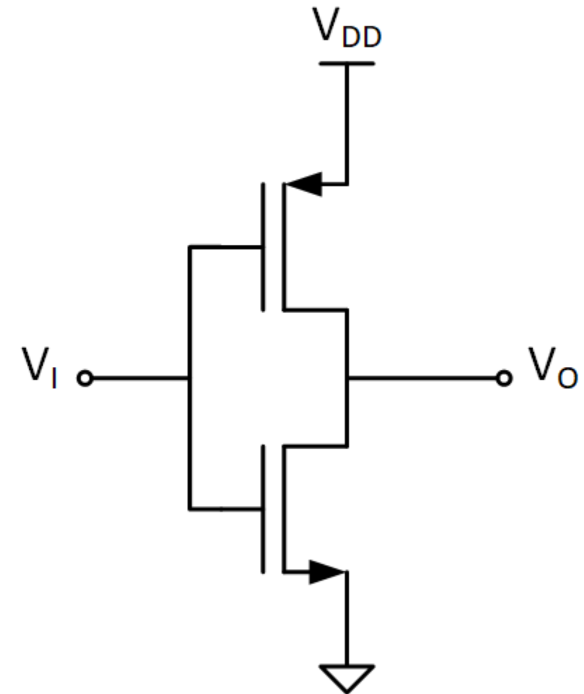
Inverters

- The ***inverter*** is a fundamental building block of ***digital logic circuits***
- Output is the ***inverse*** of the input
  - When the input is a logic high (1/T) the output is low (0/F)
  - When the input is low (0/F) the output is high (1/T)



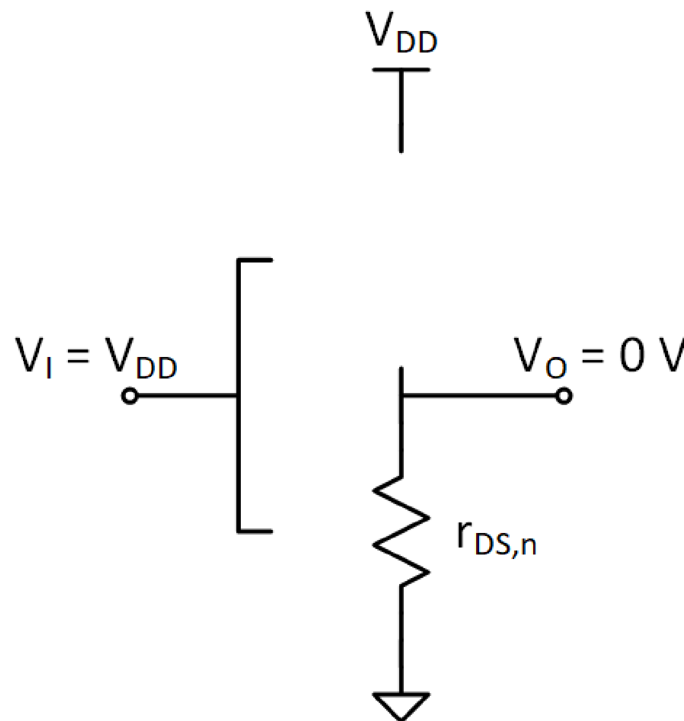
CMOS Inverter

- CMOS inverters make use of NMOS and PMOS devices acting as switches
  - Input applied to gate of each device
  - Output taken from their drain terminals
  - When one switch is on, the other is off
  - Output connected to either V_{DD} or ground



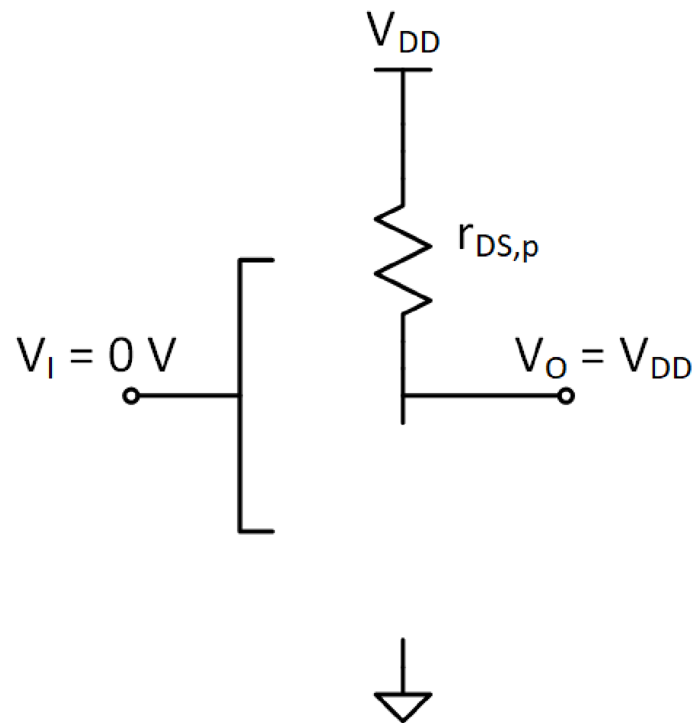
CMOS Inverter

- **<u>Input is high</u>:**
  - $V_I = V_{DD}$
  - $\left|V_{GS_p}\right| = 0\ V < \left|V_{t_p}\right|$
    - PMOS device is off
  - $V_{GS_n} = V_{DD} > V_{t_n}$
    - NMOS device is on
  - $V_O \approx 0\ V$



CMOS Inverter

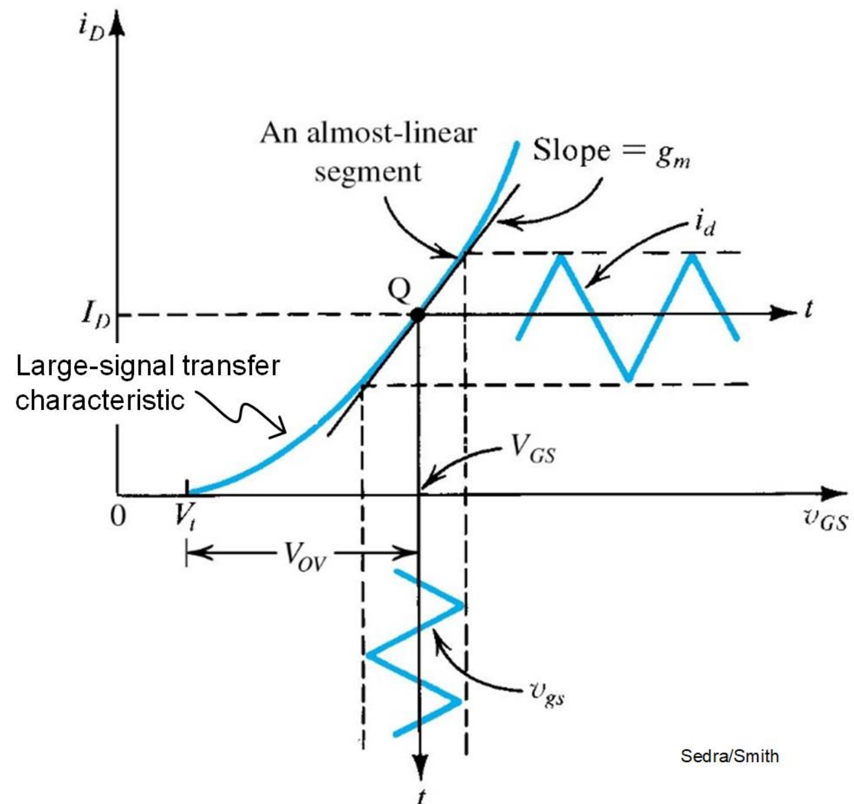
- **Input is low:**
  - $V_I = 0\ V$
  - $\left|V_{GS_p}\right| = V_{DD} > \left|V_{t_p}\right|$
    - PMOS device is on
  - $V_{GS_n} = 0\ V < V_{t_n}$
    - NMOS device is off
  - $V_O \approx V_{DD}$



Small-Signal Models

MOSFET Small-Signal Hybrid-π Model

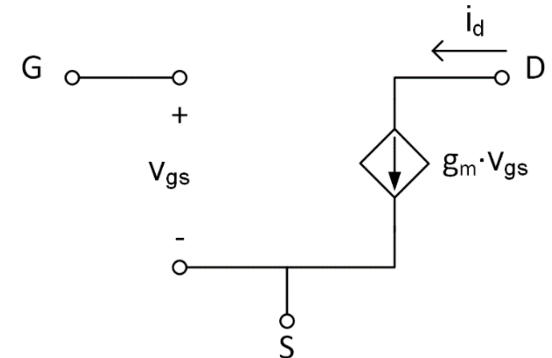
- Just as with BJTs, we use the large-signal model to determine the MOSFET's ***DC operating point***
  - DC terminal voltages and drain current
- Need a ***small-signal model*** to describes the MOSFETs response to small signals
  - To describe its behavior as an amplifier
- Small-signal model parameters determined by the DC operating point



MOSFET Small-Signal Hybrid-π Model

- Similar to the BJT hybrid-π model
  - But, input resistance at the gate is infinite:

$$i_g = 0$$



- ***Transconductance***, g_m, defined as

$$g_m \equiv \frac{\partial i_d}{\partial v_{gs}}$$

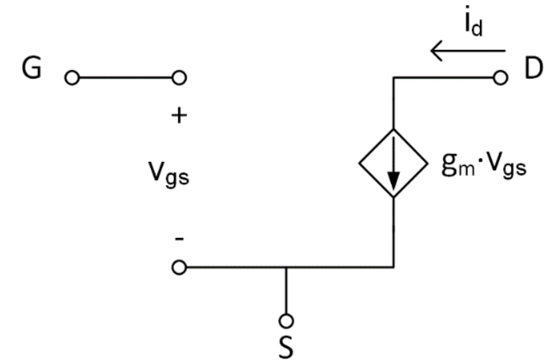
  - Where i_d and v_{gs} are the ***small-signal components*** of the drain current and gate-source voltage , respectively
- Transconductance determined by the DC operating point:

$$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{GS} - V_t)$$

$$g_m = k_n' \left(\frac{W}{L}\right) V_{OV}$$

MOSFET Small-Signal Hybrid-π Model

$$g_m = k_n' \left(\frac{W}{L}\right) V_{OV}$$



- Recall that DC drain current is given by

$$I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) V_{OV}^2$$

- Solving for V_{OV}:

$$V_{OV} = \sqrt{\frac{2I_D}{k_n' \frac{W}{L}}}$$

- Substituting the V_{OV} expression into the g_m expression:

$$g_m = k_n' \left(\frac{W}{L}\right) \sqrt{\frac{2I_D}{k_n' \frac{W}{L}}} = \sqrt{2k_n' \left(\frac{W}{L}\right) I_D}$$

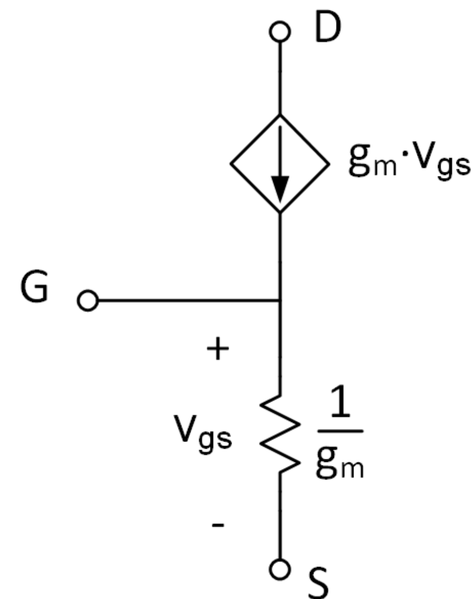
MOSFET Small-Signal T-Model

- An alternative small-signal MOSFET model is the T-model
  - As with the BJT T-model, useful when there is source resistance
- Though not immediately obvious, note that $i_g = 0$

$$i_d = i_s = g_m v_{gs}$$

- Resistance seen looking into the source:

$$R_s = \frac{1}{g_m}$$



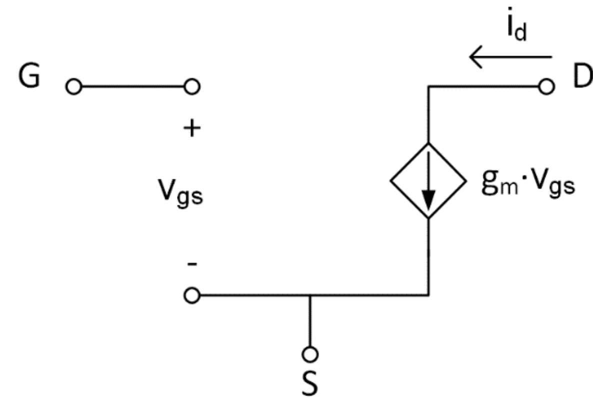
MOSFET Small-Signal Models

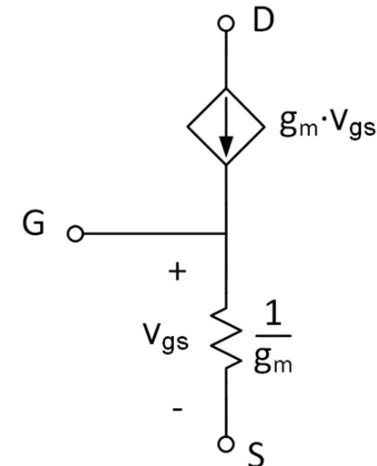
- In summary:
  - Transconductance in terms of overdrive voltage:

$$g_m = k_n' \left(\frac{W}{L}\right) V_{OV}$$

  - Transconductance in terms of drain current:

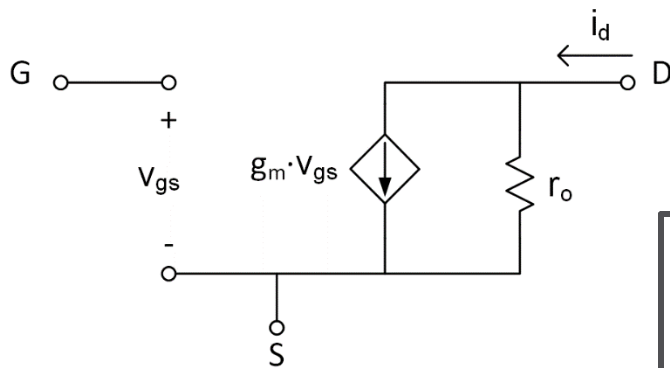
$$g_m = \sqrt{2k_n' \left(\frac{W}{L}\right) I_D}$$





Small-Signal Models – Finite r_o

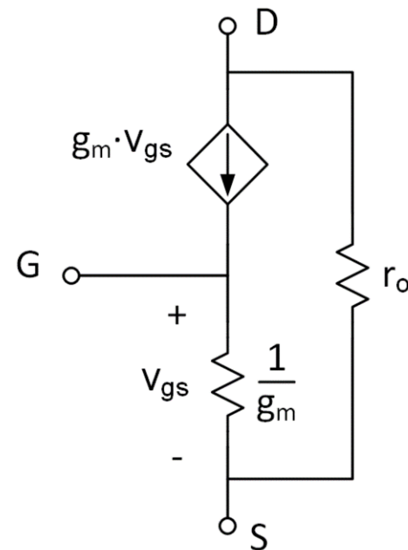
- We have seen that we can add output resistance to the large-signal model to account for channel-length modulation
  - Can do the same for the small-signal model
  - Will rarely, if ever, do this for the large signal model, but often will for the small-signal model



$$r_o = \frac{V_A}{I_D}$$

$$V_A = \frac{1}{\lambda}$$

$$I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) V_{OV}^2$$



Using the MOSFET Models

- In the next section of the course, we will look at the analysis and design of MOSFET amplifiers
  - Bias network and DC operating point
  - Signal-path
- As was the case for BJT amplifiers, our general procedure will be:
  - ***Large-signal analysis***
    - DC operating point
    - Small-signal model parameters
  - ***Small-signal analysis***
    - Circuit gain