Design and Optimization of Area-Constrained Wirelessly Powered CMOS UWB SoC for Localization Applications

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***Abstract*—This paper discusses the design of a batteryless wirelessly powered ultra-wideband (UWB) system-on-a-chip (SoC) tag for area-and-volume-constrained localization applications such as insect tracking. Key challenges for wirelessly powered operation at 10-m range include the design of high-sensitivity rectifiers and low-voltage high-efficiency UWB transmitters (TX). An antenna-rectifier co-design methodology is presented for sensitivity optimization under area constraints. A 300-nA power management unit (PMU) and low-voltage (0.8-V) UWB TX increases tag operating range by ensuring high rectifier sensitivity under loaded conditions and reducing required rectifier output voltage. The rectifier, PMU, and UWB TX are integrated in 65-nm CMOS, and the rectifier demonstrates state-of-the-art −30.7–dBm sensitivity for 1-V output voltage with only 1.3 cm^2 antenna area, representing a 2.3 × improvement in sensitivity over previously published work, at 2.6 × higher frequency with 9 × smaller antenna area, translating into a 50% longer range at the same frequency. The 0.8-V UWB TX consumes 64 pJ/pulse at 28-MHz pulse repetition rate and achieves 2.4 GHz −10-dB bandwidth. Wireless measurements demonstrate sub-10-cm range resolution at ranges exceeding 10 m. Tag measurements in typical office environments demonstrate 20-m-range RF-energy harvesting with 36-dBm effective-isotropic radiated power in the 2.4-GHz ISM band.**

***Index Terms*—Antenna, IR-UWB, localization, power management, RF energy harvesting, sensitivity, transmitter.**

I. Introduction

WIRELESSLY POWERED sensor networks are of interest for Internet-of-Things (IoT) applications due to their ability to operate without battery lifetime/replacement costs and constraints [1]–[6]. Moreover, high-levels of system-on-a-chip (SoC) integration imply that sensor tag weight, area, and volume are often limited by batteries and antennas [7]–[14]. Tracking the spatial position of miniature objects in three dimensions is important for many asset-tracking applications [15]–[19]. Spatial positioning tags are also useful in biological applications [20]–[23]—for instance, the foraging and pollination patterns of bumblebees are of great interest in the context of the key role that bees play in crop pollination and the unexplained fluctuations in bee-colony populations. Technical specifications for such insect-tracking tags are stringent, as these localization-capable sensors must achieve $<$ 10-cm resolution with extremely small form-factor and weight that minimize impact on insect flight. Similar to other volume-sensitive IoT applications, the targeted $\sim$ 100-mg weight, $<$ 1-cm dimensions, and 10-m range cannot be satisfied with batteries or piezoelectric/solar-harvesting. However, RF energy-harvesting from a beacon signal transmitted by a base-station can provide a robust, low-form factor/weight mechanism for powering the tag.

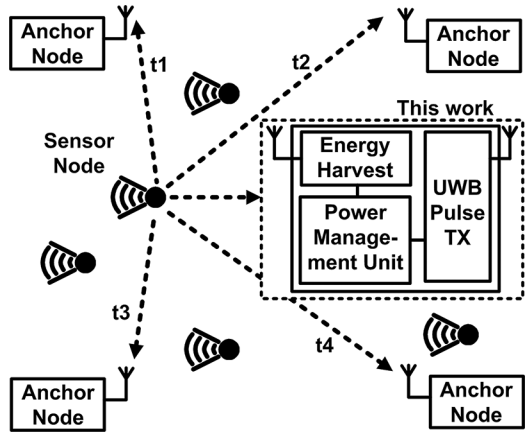

Fig. 1. Relative TDOA-based localization using wirelessly powered UWB TX SoC.

Time-difference-of-arrival (TDOA) schemes provide reliable localization performance and are less sensitive to multipath. However, TDOA localization requires triangulation based on signals received at multiple base-stations (Fig. 1) as well as wide bandwidths to achieve high resolution [24], [25]. Therefore, ultra-wideband (UWB) systems with multi-GHz bandwidths are attractive for such applications. Increasing the tag range in such schemes enables the reduction in number of base-station nodes. The maximum range of wirelessly powered UWB sensor tags is limited by either the tag rectifier sensitivity, i.e., input power required to achieve targeted output voltage, or by the signal-to-noise ratio (SNR) achieved by the sensor

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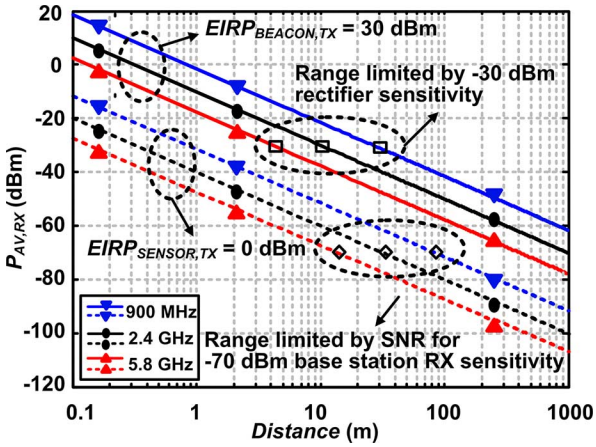

Fig. 2. Wirelessly powered sensor operating range is limited by rectifier sensitivity rather than by the SNR required for the wireless data link between the sensor and base-station.

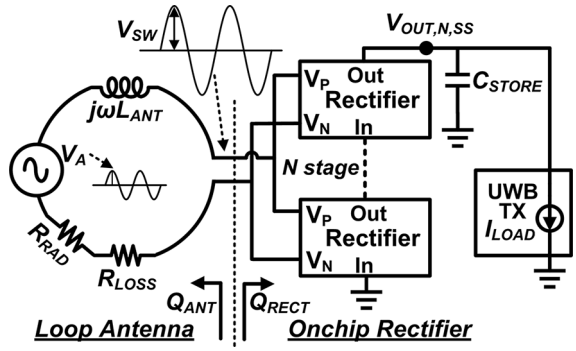

Fig. 3. Circuit and antenna model used to codesign antenna and rectifier for area-constrained sensitivity optimization.

transmitter (TX) localization signal at the base-station receiver (RX). As shown in Fig. 2 [26], even if state-of-the-art rectifier sensitivity of -30 dBm and beacon TX effective isotropic radiated power (EIRP) of 1 W are assumed, the sensor tag range is limited by rectifier sensitivity rather than by sensor SNR at the base-station for typical applications. While range can be improved with higher sensor tag antenna gain, this reduces the tag field-of-view and causes an undesirable increase in tag size. Therefore, rectifier sensitivity optimization is critical for increasing sensor operating range.

A wirelessly powered UWB SoC with rectifier–antenna codesign for sensitivity optimization was presented in [27], and system-level tradeoffs/approaches in the context of insect-localization application were described in [26]. In this paper, we present further details of the optimization approach underlying the codesign of the antenna and rectifier for area-constrained localization applications. A charge-conservation-based one-stage model that enables faster estimation of rectifier output voltage and charging times is also described in Section II. The one-stage model is used in the systematic codesign approach, detailed in Section II, that leads to state-of-the-art rectifier performance given area constraints. From a system perspective, rectifier sensitivity can also be improved by reducing rectifier load current and targeted output voltage. Section III details the design of the power-management unit (PMU) in [27] and presents the 8-GHz UWB pulse generation and PA design approach that operates with 0.8-V supply and directly matches UWB TX output to a compact loop antenna. Section IV describes the measured performance of the wirelessly powered UWB SoC including rectifier and UWB antennas, demonstrating state-of-the-art performance at range exceeding 10 m. Conclusions and areas of future research are discussed in Section V.

II. Antenna–Rectifier Codesign for Area-Constrained Applications

A. Weight/Area Budget and Design Challenges

Our objective is a positioning sensor that is so small and lightweight that it permits insect flight with the sensor attached. This application limits sensor weight and size, precluding the use of commercial batteries. On the other hand, RF energy harvesting from a beacon signal is lightweight since it only requires an antenna and is reliable if RF energy is present. Total sensor tag weight is targeted to be < 100 mg—individual component weights are detailed in Section IV.

For the RF-energy harvesting system, rectifier sensitivity in order to achieve a targeted operating range for rectifier output voltage sets for a given TX EIRP (Fig. 2). In the ISM band, the EIRP is limited to 4 W when antenna gain is less than 6 dBi [28]. Since the input power at the antenna is a function of path loss, the range increases for lower frequencies that have lower path loss (Fig. 2). However, lower frequencies result in antenna area larger than the targeted 1 cm^2. Based on iteration through the design procedure outlined in following sections for ISM frequencies at 900 MHz, 2.4 GHz, and 5.8 GHz, we target 2.4-GHz operation to balance antenna size and path loss.

B. Rectifier State of the Art

The RF energy available to the rectifier $P_{\mathrm{AV,RX}}$ can be obtained from [29]

$$P_{\mathrm{AV,RX}} = \mathrm{EIRP_{TX}} \left(\frac{\lambda}{4\pi d}\right)^2 G_{\mathrm{RX}} \tag{1}$$

where G_{RX} is RX antenna gain, λ is the wavelength, and d is TX–RX separation. High path loss at GHz frequencies requires the rectifier to operate from μW signal levels—for example, 1-W TX EIRP at 2.4 GHz with 10-m TX-RX separation leads to 1-μW $P_{\mathrm{AV,RX}}$ for isotropic RX antenna. In the following, the energy-harvesting rectifier sensitivity is defined in terms of the power available to an isotropic RX antenna, $P_{\mathrm{AV,RX,ISO}}$ [assuming $G_{\mathrm{RX}} = 1$ in (1)] [30].

As shown in Fig. 3, the steady-state output voltage in an N-stage rectifier, $V_{\mathrm{OUT,N,SS}}$,

$$V_{\mathrm{OUT,N,SS}} = N(V_{\mathrm{SW}} - V_D) \tag{2}$$

depends upon the input voltage swing V_{SW}, the rectifier drop voltage V_D, which is also a function of V_{SW}, the transistor threshold voltage V_{TH} and the load resistance R_{LOAD}. *The objective of rectifier design is to minimize the $P_{\mathrm{AV,RX,ISO}}$ required to achieve a targeted $V_{\mathrm{OUT,N,SS}}$.*

A lower V_{TH} results in a lower V_D and reduces required V_{SW}. Therefore, several research efforts have focused on reducing effective V_{TH} to improve sensitivity. Rectifiers with zero-V_{TH}

transistors have demonstrated −26.4-dBm sensitivity for 1-V output at 915 MHz [31]. Notably, improvements provided by zero-$V_{\rm TH}$ threshold are at the cost of increased number of fabrication masks and are limited by higher leakage in the transistors. Floating-gate devices have been proposed that reduce rectifier threshold voltage using passive means [32]. However, this strategy requires a pre-biasing scheme to inject charge on the floating gate to reduce the threshold. Internal threshold compensation can also reduce effective $V_{\rm TH}$ [33]. However, this increases input rectifier capacitance which degrades sensitivity, as discussed in Section II-F. Rectifier design in subthreshold has been analyzed in [34], leading to −32-dBm sensitivity with 50 stages. However, the resulting capacitance limits the use of electrically small antennas at high frequencies.

Codesign of antenna and rectifier has been proposed for maximizing $V_{\rm OUT,N,SS}$ by increasing $V_{\rm SW}$ for a given $P_{\rm AV,RX,ISO}$ in [30]. Such design techniques can potentially balance tradeoffs between antenna, matching network, rectifier architecture, and sizing to optimize $V_{\rm OUT,N,SS}$. The device dimensions in [30] are chosen mainly based on charging time optimization which is a weak function of transistor sizing for large widths. Additionally, the antenna used in [30] occupies 12 cm^2 making it unsuitable for small tags. Here, we extend the approach in [30] by proposing a systematic methodology to determine rectifier device sizing, number of stages as well as area-constrained antenna design methodology that leads to state-of-the-art rectifier sensitivity and therefore a significant increase in energy-harvesting range.

C. Model for Rectifier–Antenna Codesign

The input-swing $V_{\rm SW}$ at the antenna can be computed based on the model in Fig. 3, where the antenna is modeled as a voltage source in series with the radiation resistance, $R_{\rm RAD}$ and loss $R_{\rm LOSS}$ of the antenna. The rectifier's input impedance is capacitive and can be modeled as a resistor $R_{\rm RECT}$ in series with a capacitor $C_{\rm RECT}$.

A high passive-boost translates a small input swing V_A to a high voltage swing at the rectifier input $V_{\rm SW}$. Matching the antenna directly to the rectifier input is desirable to avoid losses due to any additional passive components that realize the network. Since the rectifier is capacitive, an inductive antenna impedance is assumed in Fig. 3 [30]. Therefore, the effective quality factor (Q) of the network $Q_{\rm EFF}$ is given by

$$\frac{1}{Q_{\rm EFF}} = \frac{1}{Q_{\rm ANT}} + \frac{1}{Q_{\rm RECT}} \tag{3}$$

and, for high $Q_{\rm EFF}$, assuming antenna and rectifier resonance, we have

$$V_{\rm SW} = Q_{\rm EFF} \cdot \sqrt{8 P_{\rm AV,RX,ISO} R_{\rm ANT} \eta_{\rm ANT}} \tag{4}$$

where $R_{\rm ANT} = R_{\rm RAD} + R_{\rm LOSS}$ and $\eta_{\rm ANT} = R_{\rm RAD}/R_{\rm ANT}$.

The antenna and rectifier parameters are related to targeted output voltage through (2) and (4), which serves as the basis for minimizing $P_{\rm AV,RX,ISO}$ in the following sections.

D. Multistage Rectifier Design

Design parameters for a multistage rectifier in Fig. 4 include the number of stages N, as well as rectifier device geometry (W/L). Given the settling time associate with storage capacitor $C_{\rm STORE}$ and the current $I_{\rm LOAD}$ (Fig. 3), rectifier design often involves long transient simulations with time steps dictated by the input RF frequency. Multiple rectifier stages further increase design complexity and simulation time. Therefore, a scalable model that predicts N-stage rectifier behavior based on one-stage rectifier simulations can considerably simplify rectifier design while providing key insights.

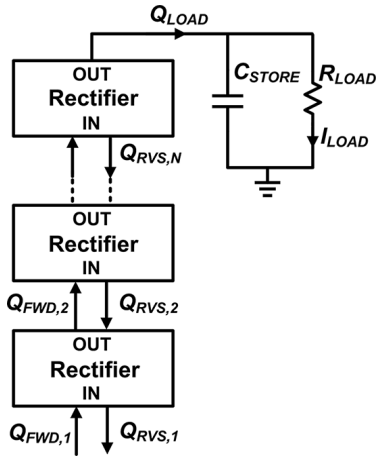

Fig. 4. Charge transfer in the steady state in an N-stage rectifier.

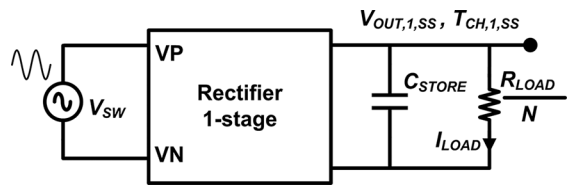

Fig. 5. One-stage equivalent model to estimate N-stage steady-state output, $V_{\rm OUT,N,SS}$, and settling time for a given input swing, $V_{\rm SW}$.

In the steady state, the capacitor dissipates a charge $Q_{\rm LOAD}$ due to the load current $I_{\rm LOAD}$ in each RF cycle, and hence the rectifier stages must replenish $Q_{\rm LOAD}$ on the storage capacitor. Fig. 4 outlines the charge transfer between multiple rectifier stages in each cycle. Ignoring leakage to the substrate, charge conservation requires that

$$Q_{\rm FWD,k} - Q_{\rm RVS,k} = Q_{\rm FWD,k+1} - Q_{\rm RVS,k+1}, \quad \text{for } 1 \le k \le N-1 \tag{5}$$

$$Q_{\rm FWD,N} - Q_{\rm RVS,N} = Q_{\rm LOAD} \tag{6}$$

$$\text{Therefore, } Q_{\rm FWD,N} = Q_{\rm LOAD} + Q_{\rm RVS,1}. \tag{7}$$

Hence, *each rectifier-stage current is the same, with the current compensating the charge loss due to $I_{\rm LOAD}$ and N-stage rectifier leakage currents.* This leads to the equivalent one-stage rectifier model in Fig. 5, which has the same load current as the N-stage rectifier and can accurately estimate performance with faster simulations, as discussed below.

From (2), predicting $V_{\rm OUT,N,SS}$ requires V_D. While the subthreshold model used in [34] can be used to calculate V_D from closed-form equations, [34] assumes no $I_{\rm LOAD}$. The finite load current due to the PMU implies that even in subthreshold, the

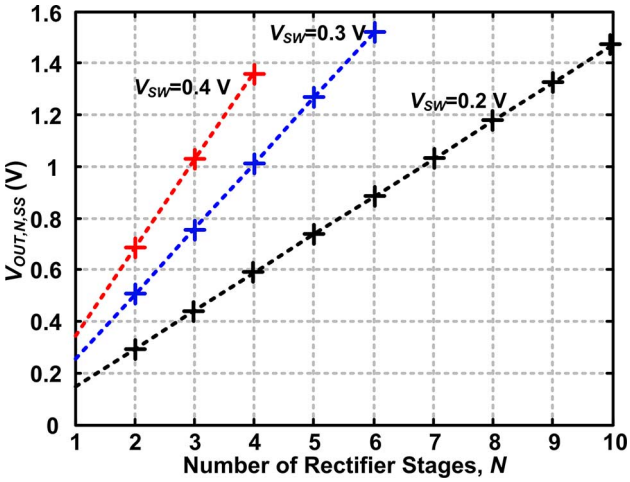

Fig. 6. Comparison between simulated $V_{\mathrm{OUT,N,SS}}$ and estimated $N \cdot V_{\mathrm{OUT,1,SS}}$ from one-stage model shows accuracy of approach.

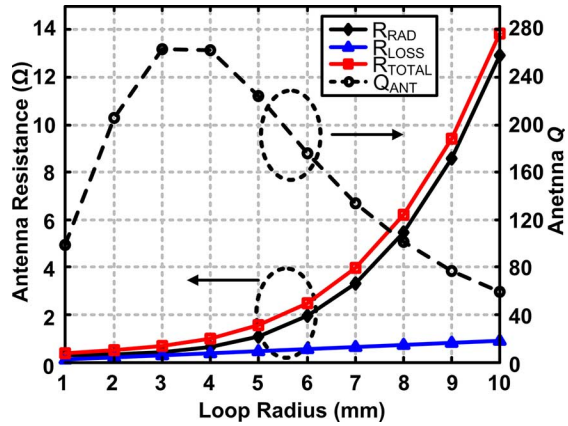

Fig. 7. Loop antenna parameters at 2.4 GHz used in the model in Fig. 3.

rectifier voltage drop V_D is affected by V_{TH} and W. Therefore, simulations are required to accurately estimate V_D. The one-stage model in Fig. 5 can be used to accurately determine V_D for a given V_{SW} from simulated $V_{\mathrm{OUT,1,SS}}$ as follows:

$$V_D = V_{\mathrm{SW}} - V_{\mathrm{OUT,1,SS}} \tag{8}$$

and N-stage output can be simply calculated from (2) and (8) for the model in Fig. 3. Hence, the one-stage model enables the V_D for the N-stage rectifier to be determined from faster one-stage rectifier simulations.

Fig. 6 validates the assumption of negligible substrate leakage in (7), where the impact of leakage due to higher voltages in N-stage rectifiers is ignored. The simulated N-stage rectifier $V_{\mathrm{OUT,N,SS}}$ shown in dashed line matches estimation using one-stage simulations for different N and V_{SW}.

The required $P_{\mathrm{AV,RX,ISO}}$ for a targeted N-stage output voltage $V_{\mathrm{OUT,N,SS}}$ can be determined from (2), (4), and (8) as follows:

$$P_{\mathrm{AV,RX,ISO}} = \frac{1}{8R_{\mathrm{RAD}}Q_{\mathrm{EFF}}^2}\left(\frac{V_{\mathrm{OUT,N,SS}}}{N} + V_D\right)^2 \tag{9}$$

and the rectifier operating range d_{RECT} can be computed from (1) and (9) as follows:

$$d_{\mathrm{RECT}} = \frac{\lambda}{4\pi}\sqrt{\frac{\mathrm{EIRP_{TX}}}{P_{\mathrm{AV,RX,ISO}}}}. \tag{10}$$

As will be described in the following, the one-stage model can also be used to estimate charging times and simplifies systematic rectifer–antenna codesign and optimization.

E. Rectifier Charging-Time Estimation Model

Charging time $T_{\mathrm{CH,N,SS}}$, of the N-stage rectifier is also an important parameter in some applications. It is defined as the 10%–90% time that the storage capacitor needs to reach steady state voltage $V_{\mathrm{RECT,SS}}$ and is dependent on rectifier and the load. From charge-transfer perspective, the charge transferred to the load in the one-stage case in each cycle is the same as in the N-stage case (Fig. 5). Since the N-stage case has N times higher voltage on C_{STORE}, it takes N times longer to achieve the steady state in the N-stage case. A similar argument can also be constructed based on the N-times smaller effective load resistance for the one-stage model, implying N times larger charging time constant. Hence, the N-stage charging time $T_{\mathrm{CH,N,SS}}$ can be estimated from one-stage charging time $T_{\mathrm{CH,1,SS}}$ as

$$T_{\mathrm{CH,N,SS}} = NT_{\mathrm{CH,1,SS}}. \tag{11}$$

F. Rectifier–Antenna Codesign Approach

As discussed in Section II-C, directly resonating the antenna and the rectifier avoids losses associated with additional matching components. For resonance, we have

$$\omega L_{\mathrm{ANT}} = \frac{1}{\omega C_{\mathrm{RECT}}}. \tag{12}$$

The model for the loop antenna wire radius b and loop radius a corresponding to Fig. 3 is given by [35]

$$L_{ANT} = \mu a\left(\ln\left(\frac{8a}{b}\right) - 2\right) \tag{13}$$

$$R_{\mathrm{RAD}} = 31171\left(\frac{\pi a^2}{\lambda^2}\right)^2$$

$$R_{\mathrm{LOSS}} = \frac{a}{b}\sqrt{\frac{2\pi f\mu}{\sigma}}. \tag{14}$$

The quality factor of the antenna is therefore

$$Q_{\mathrm{ANT}} = \frac{\omega L_{\mathrm{ANT}}}{R_{\mathrm{RAD}} + R_{\mathrm{LOSS}}}. \tag{15}$$

Fig. 7 plots R_{RAD}, R_{LOSS}, R_{TOTAL},and Q_{ANT} of a loop antenna at 2.4 GHz as a function of loop radius for wire radius $b = 250$ μm. Notably, R_{RAD} increases faster compared with R_{LOSS} as the loop circumferences gets closer to $\lambda/2$, leading to higher loop-antenna efficiency. However, as loop size becomes larger, R_{RAD} increases faster than the reactance, resulting in lower Q_{ANT}. Since (9) shows that the output voltage depends on R_{RAD} as well as Q_{ANT}, optimum sensitivity is achieved by

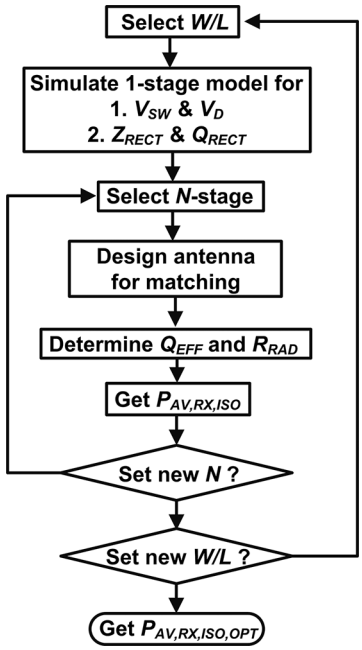

Fig. 8. Systematic rectifier–antenna codesign for optimizing rectifier sensitivity.

balancing these tradeoffs. Fig. 8 outlines the proposed systematic area-constrained antenna–rectifier codesign approach.

1) Rectifier–Antenna Codesign Procedure:

1) For a given rectifier device geometry W/L, the one-stage model is used to determine V_D as a function of $V_{\rm SW}$. The large-signal input impedance of the one-stage rectifier for $V_{\rm SW}$ is computed using Fourier transform of the steady-state rectifier current, where

$$Z_{\rm RECT} = \frac{V_{\rm SW}}{Fund\left(\mathrm{FFT}\left(I_{\rm RECT}\left(t\right)\right)\right)}. \tag{16}$$

2) For each N of interest, one-stage V_D can be used to estimate $V_{\rm SW,MIN}$, which is the minimum required $V_{\rm SW}$ to achieve targeted steady-state output voltage $V_{\rm OUT,N,SS}$. N-stage rectifier input impedance is computed from

$$R_{\rm RECT,SS} = \frac{R_{\rm 1STG,SS}}{N} \tag{17}$$

$$C_{\rm RECT,SS} = N\, C_{\rm 1STG,SS} \tag{18}$$

$$Q_{\rm RECT,N} = \frac{1}{\omega\left(C_{\rm RECT,SS} + C_{\rm PAR,N}\right) R_{\rm RECT,SS}} \tag{19}$$

where $C_{\rm PAR,N}$ represents the layout-dependent input wiring and pad parasitic capacitances ($\sim$ 100 fF).

3) Given N-stage input impedances, (12) and (13) determine loop antenna size. Therefore, R_{RAD} and Q_{ANT} can be computed from (15).
4) Following this, the required $P_{AV,RX,ISO}$ to achieve $V_{OUT,N,SS}$ for the given W/L and N can be determined from (9). The procedure is iterated across multiple stage number N and devices sizes to determine the minimum sensitivity.

This design procedure is summarized in Fig. 8 and is adopted in order to codesign a 2.4-GHz rectifier and loop antenna in 65-nm CMOS, with loop antenna radius limited to 6.5 mm.

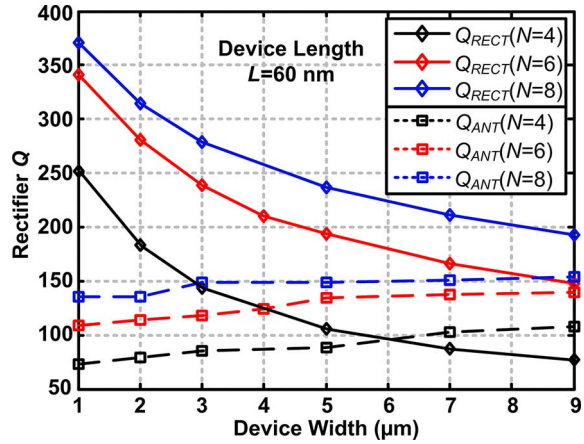

Fig. 9. Rectifier and antenna quality factors following codesign approach in Fig. 8, satisfying 1-V output voltage target.

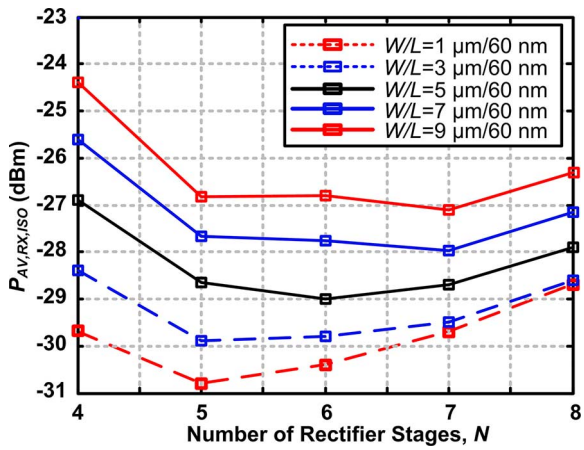

Fig. 10. Required $P_{\rm AV,RX,ISO}$ to achieve targeted 1-V output voltage across device width and number of rectifier stages.

Given (12) and (13), this sets a lower bound on $C_{\rm RECT}$ and hence limits the permissible combinations of N and W/L. Differential cross-connected rectifier topology is adopted since it effectively reduces turn-on voltage[30]. Minimum channel length is chosen for all transistors to minimize device capacitances.

Fig. 9 shows the antenna and rectifier Q at 2.4 GHz across W for different N, assuming a 1-V $V_{\rm OUT,N,SS}$ target, $I_{\rm LOAD}$ = 100 nA, and resonance between loop antenna and rectifier. Increasing W leads to higher $C_{\rm RECT}$ and a steep reduction in $Q_{\rm RECT}$, and gradual increase in $Q_{\rm ANT}$ as loop antenna radius decreases. Larger N leads to higher $Q_{\rm RECT}$ due to presence of wiring and pad parasitics [$C_{\rm PAR,N}$ in (19)] that do not scale with N. The increase in $C_{\rm RECT}$ for larger N also leads to smaller antenna size and higher $Q_{\rm ANT}$. As described earlier, smaller antenna size leads to poorer $R_{\rm RAD}$ that degrades sensitivity.

The overall impact of these tradeoffs is shown in Fig. 10, which plots the sensitivity following the design procedure in Fig. 8. A small device size with $N = 5$ provided the optimum sensitivity in simulation but can lead to long charging time. Increasing the device width in the rectifier leads to faster charging times. In order to balance sensitivity with practical charging

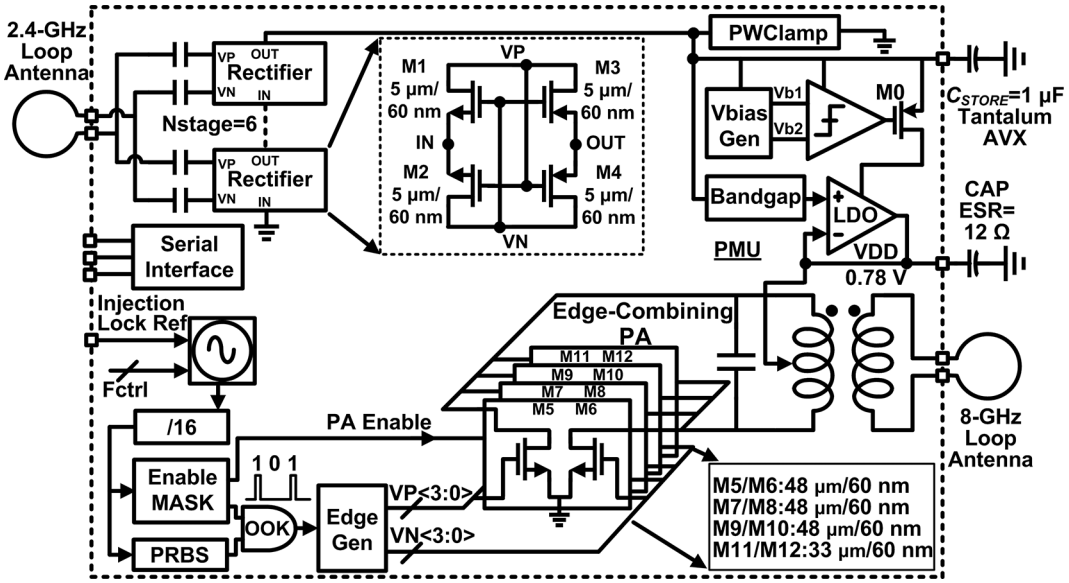

Fig. 11. Wirelessly powered UWB TX SoC with 2.4-GHz rectifier, low-current PMU, and 0.8-V 8-GHz UWB TX.

time, a choice $N = 6$ with $W = 5$ μm is selected for this design since it reduces charging time by factor of three, albeit with a $\sim$ 1.8-dB poorer simulated sensitivity. The loop antenna corresponding to the selected rectifier size presents a simulated impedance of $2 + j260$ Ω at the rectifier input, resonating rectifier capacitance. Including the rectifier, the simulated $Q_{\rm EFF}$ is $\sim$70 based on (3), corresponding to a bandwidth of $\sim$ 30 MHz. This approach of directly resonating antenna and rectifier does present smaller bandwidths since high-Q passive boost is targeted, however calibration (similar to [30]) can be used to ensure rectifier operation at desired frequency.

A similar optimization approach is carried out at 900 MHz with the same antenna area constraint to determine the minimum $P_{\rm AV,RX,ISO}$ and hence the rectifier operating range. Based on these simulations, an operating frequency of 2.4 GHz was selected for RF-energy harvesting.

III. Wirelessly Powered UWB TX SoC

The wireless-energy rectifier outlined in Section II is used to power a UWB TX sensor node SoC shown in Fig. 11. Duty-cycled operation is assumed where the rectifier charges a capacitance, ($C_{\rm STORE}$ in Fig. 11), and the UWB TX is enabled only when sufficient voltage has been built up on the capacitor. The UWB TX hence operates in bursts which is suited for low-data-rate sensors which do not require continuous transmission. Low-voltage operation is targeted to improve rectifier operating range. The sensor node consists of three integrated blocks: the RF energy harvester, PMU, and UWB transmitter. In power-up mode, wireless TX power from an external 2.4-GHz beacon is harvested and stored on capacitor $C_{\rm STORE}$. A low-current PMU, based on a subthreshold bandgap reference, detects when the voltage on the storage capacitor $V_{\rm RECT,N,SS}$ exceeds a programmable threshold (nominally 1.1 V), after which the low-dropout regulator (LDO) is enabled and provides a constant supply voltage (nominally 0.78 V) to the UWB TX. The 0.8-V UWB TX operates in the higher UWB band with center frequency at 8 GHz to ensure multi-GHz bandwidth with a compact loop antenna.

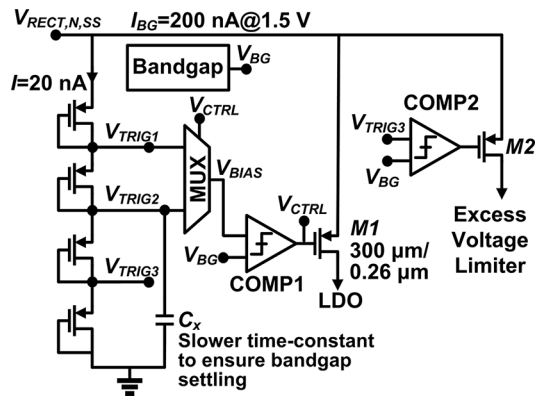

Fig. 12. Schematic of programmable PMU that draws $<$ 300 nA.

A. Power Management Unit

The PMU is shown in Fig. 12. The rectifier output voltage $V_{\rm RECT}$ powers a bandgap circuit biased in subthreshold region[36]. The bandgap circuit consumes 150 nA when $V_{\rm RECT} = 1.5$ V. The simulated variation in V_{BG} across 0° to 50° is 5 mV. The bandgap circuit requires a $V_{\rm RECT} > 0.5$ V to achieve stable output voltage

1) Charging Phase: Diode-connected transistor ladder scales the input voltage $V_{\rm RECT}$ to different levels. Initially, $V_{\rm BIAS}$ is connected to $V_{\rm TRIG2}$ since $V_{\rm CTRL}$ is low. A comparator $COMP1$ compares $V_{\rm BIAS}$ and the bandgap output voltage $V_{\rm BG}$. As $V_{\rm RECT}$ increases, $V_{\rm BIAS}$ increases, and, hence, $COMP1$ toggles $V_{\rm CTRL}$ to high. While this nominally occurs when $V_{\rm RECT,N,SS} > 1.1$ V, $V_{\rm TRIG2}$ and hence $V_{\rm CTRL} \rightarrow 1$ is programmable. When $V_{\rm BIAS}$ exceeds $V_{\rm BG}$, $V_{\rm CTRL}$ enables the switch M_1, and the LDO is activated to provide a stable supply voltage for the UWB transmitter. At the same time, $V_{\rm BIAS}$ is switched to higher $V_{\rm TRIG1}$.

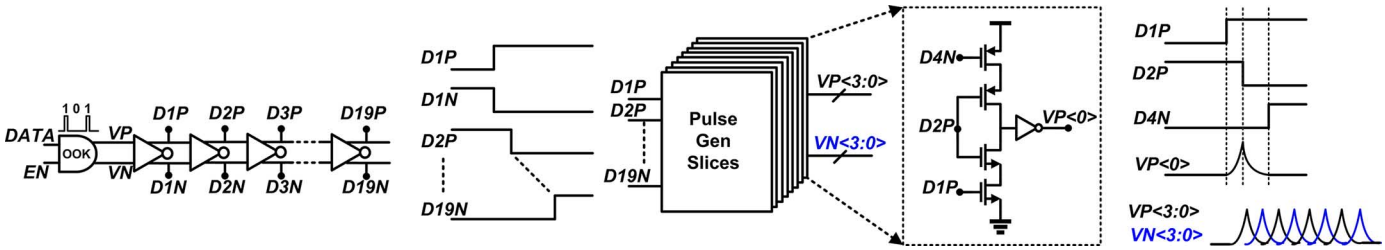

Fig. 13. Generation of UWB pulse with 500-ps pulse width and 8-GHz center frequency using edge combining.

2) Discharging Phase: The UWB-TX current discharges capacitor $C_{\rm STORE}$ and hence $V_{\rm BIAS}$. When $V_{\rm BIAS}$ is lower than $V_{\rm BG}$ (normally when $V_{\rm RECT}$ is lower than 0.78 V), $COMP1$ toggles $V_{\rm CTRL}$ to low. Switch M_1 is turned off, and the LDO is deactivated. The system returns to charging phase. Additionally, when $V_{\rm RECT}$ exceeds 1.8 V, $COMP2$ turns on M_2 to provide a current discharge path to ground, limiting $V_{\rm RECT,N,SS}$ and preventing breakdown.

B. UWB Pulse Generation

A four-stage differential ring oscillator, tunable from 100 to 400 MHz, provides the clock for the UWB TX (Fig. 11). The oscillator can also be injection-locked to an external input, enabling synchronization with other sensor nodes or base station. The ring oscillator clock is divided by 16 to generate the data clock, leading to on–off keying (OOK) modulated UWB pulses at data rates between 6–28 Mb/s.

An on-chip pseudo-random bit-sequence (PRBS) generator is used to emulate coding on the sensor-tag pulses for individual tag identification. OOK modulation is adopted to ensure low-voltage pulse generation. Data are provided to a programmable current-starved delay chain in Fig. 13 that generates edges delayed by 62.5 ps in the case of the Data "1" state. Pulses are created by combining suitable delay edges. For example, delayed edges $D1P$, $D2P$, and $D4N$ are fed to the edge-combine branch to generate $VP\langle 0\rangle$. Similarly, pulses $VP\langle 3:0\rangle$ (black) and $VN\langle 3:0\rangle$ (blue) are generated based on other edges of the inverter delay chain, creating eight pulses each with duration of 62.5 ps (Fig. 13). The choice of OOK modulation with an enable mask reduces the number of stacked devices in the pulse generator to four instead of six in [37], enabling 62.5-ps pulse generation from as low as a 0.7-V supply.

C. PA Antenna Codesign

The PA combines the VP and VN pulses from Fig. 13, creating a UWB pulse with 8-GHz center frequency and 500-ps duration (Fig. 11). The PA provides pulse-shaping for the UWB TX output by utilizing weighted transconductances and targets 0-dBm output power, consuming 14 mW when amplifying a pulse. The PA is duty-cycled by creating a PA-Enable mask (Fig. 11) that activates the PA when a pulse needs to be transmitted. The width of the PA-Enable signal is programmable to ensure appropriate settling time for the PA.

Differential operation for the TX is critical due to the limited bypass and small ground plane of the area-constrained sensor. In this work, differential PA output-impedance matching to the antenna is achieved using an area-efficient transformer-capacitor network that incorporates wirebonds, as shown in Fig. 14. The transformer also separates voltage bias of the PA from antenna. The transformer primary coil and secondary coil are implemented with metal 9 and metal 8 stacked together, occupying an area of 178 μm$\times$ 200 μm. EM simulations, performed using Hyperlynx 3D EM (version 15), show transformer primary and secondary inductances of 340 and 360 pH, respectively, with a coupling factor of $\sim$ 0.8. The PA is matched to a compact 8-GHz loop antenna which is designed to resonate with bond-wire inductance. With an outer radius of only 0.57 cm, the loop antenna exhibits simulated impedance of $55\ \Omega - j112\ \Omega$ at 8 GHz. The transformer-capacitor network is designed such that the PA creates a 0-dBm swing across the antenna radiation resistance.

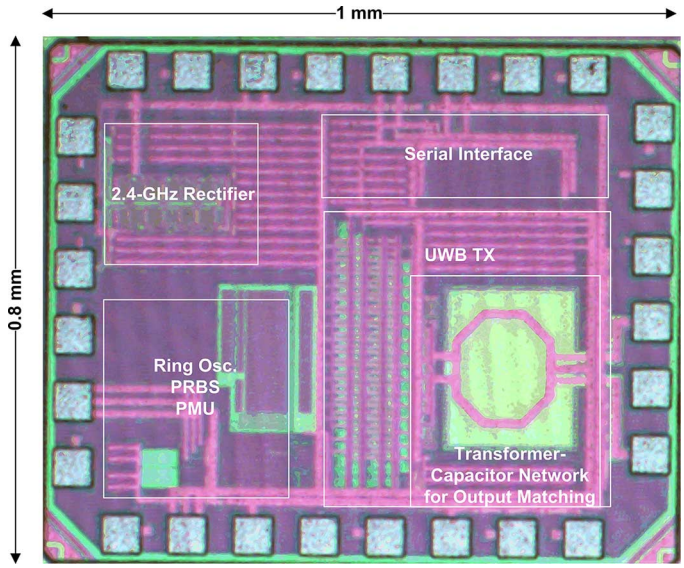

Fig. 14. Die photograph of wirelessly powered 8-GHz UWB TX implemented in 65-nm CMOS.

IV. Measurement Results

The wirelessly powered 8-GHz UWB TX SoC is implemented in a 65-nm CMOS process with 3.4-μm-thick top-layer metal. The die area is 1 mm $\times$ 0.8 mm, as shown in Fig. 14. The only off-chip components are compact loop antennas, surface mount (SMT) storage capacitor, and LDO stability capacitors, all of which have very small form factor. A compact chip-on-board package for RF testing is shown in Fig. 15(a). A simulated rectifier antenna pattern, using Ansys High Frequency Structure Simulator (HFSS) (version 15), is shown in Fig. 15(b), demonstrating a gain of $\sim$ 1.1 dBi with 90%

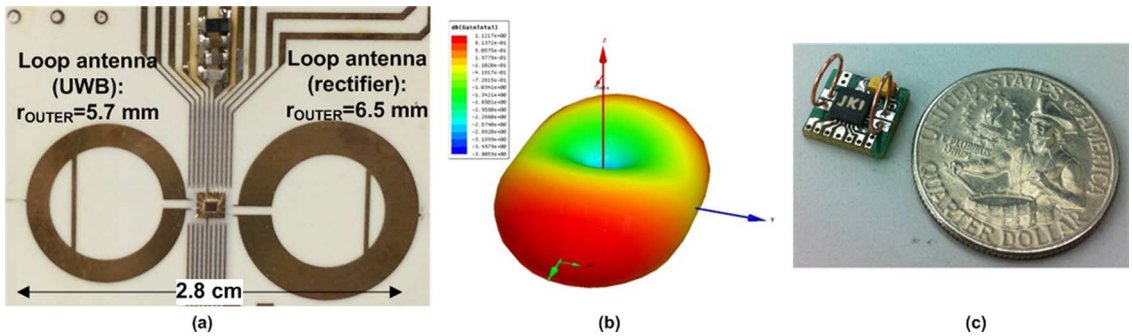

Fig. 15. (a) UWB SoC packaged with dual planar loop-antennas for RF testing. (b) Simulated 2.4-GHz loop antenna gain. (c) Compact 3-D package for low form-factor and weight.

TABLE I
COMPONENT MASS SUMMARY

Component	Mass	Component	Mass
Flex PCB (1 cm^2)	20 mg	Cu Wire (24 AWG, 2 cm)	38 mg
Tantalum Cap. (1 μF)	28 mg	0603 SMT Cap.	3.6 mg

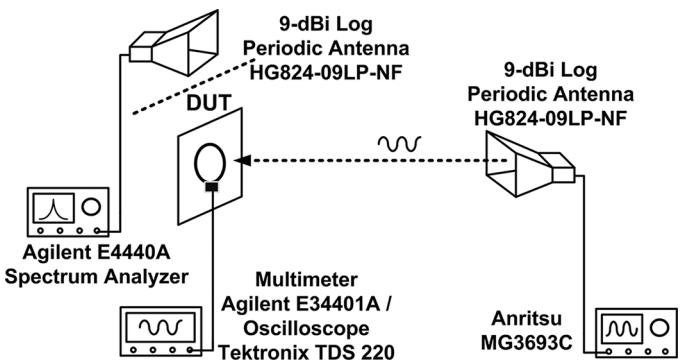

Fig. 16. Measurement setup for characterizing rectifier performance—setup is initially calibrated to determine available power for the rectifier.

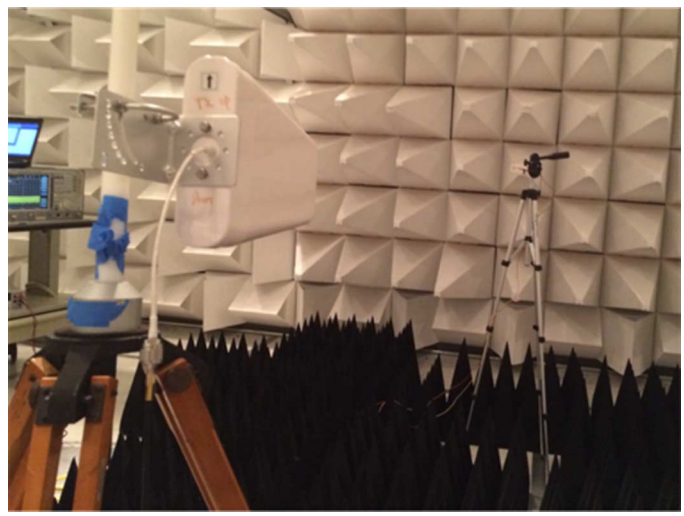

Fig. 17. Photograph of a 2.4-GHz rectifier–antenna measurement in an anechoic chamber.

efficiency. Similar gain performance is observed for the 8-GHz UWB antenna with both antennas demonstrating low gain and wide field-of-view. The radius of the 2.4-GHz rectifier antenna is comparable to that of the 8-GHz UWB antenna since the inductive antenna is used to directly resonate the resonator, as was described in Section II-F. While the planar chip-on-board package is used for systematic testing, a small form-factor package with FR-4 as well as flex-PCB with vertical loop antennas has also been developed, as shown in Fig. 15(c). Typical component weights contributing to overall $\sim$ 100-mg sensor tag weight are shown in Table I.

Rectifier measurements are carried out both in an anechoic chamber and in typical office environments. Wireless UWB TX performance is measured both in time and frequency domains. Relative time-of-flight (TOF) measurements demonstrate localization capabilities.

A. Rectifier–Antenna Performance

The rectifier measurement is calibrated using two identical 9-dBi-gain log-periodic antennas, as shown in Fig. 16. The rectifier sensitivity is defined as the available power $P_{\mathrm{AV,RX,ISO}}$ from an isotropic receiving antenna with impedance and polarization matching, which can be determined from the setup in Fig. 16. The measured $P_{\mathrm{AV,RX,ISO}}$ is consistent with the calculated received power from (1), validating setup calibration. The rectifier and antenna are characterized in an anechoic chamber as shown in Fig. 17. Sensitivity and charging transients under three load conditions of $R_{\mathrm{LOAD}} = \infty$, 10 M$\Omega$, and 1 M$\Omega$ were measured. As shown in Fig. 18(a), the implemented rectifier–antenna achieves state-of-the-art -30.7-dBm sensitivity for 1-V output voltage. Notably, this performance is achieved with only $\sim$ 1.3-cm^2 of antenna area demonstrating the validity of the proposed optimization based on rectifier–antenna codesign. The measurements agree well (within 1 dB) with simulations in Fig. 10, and the relatively small difference (1 dB) between simulation and measurement most likely comes from inaccurate transistor models at subthreshold region (where rectifier transistors operate at sensitivity) and wirebond/antenna modeling inaccuracies. Fig. 18(b) shows the measured charging time under both 10 MΩ and 1 MΩ load when charging a 1-uF tantalum storage capacitor to 1-V $V_{\mathrm{RECT,SS}}$. Rectifier power conversion efficiency (PCE) is defined as

$$\mathrm{PCE} = \frac{P_{\mathrm{LOAD}}}{P_{\mathrm{AV,ISO}}} \tag{20}$$

where P_{LOAD} is the power dissipated in the load resistance. Fig. 18(c) shows measured PCE under both 10- and 1-MΩ

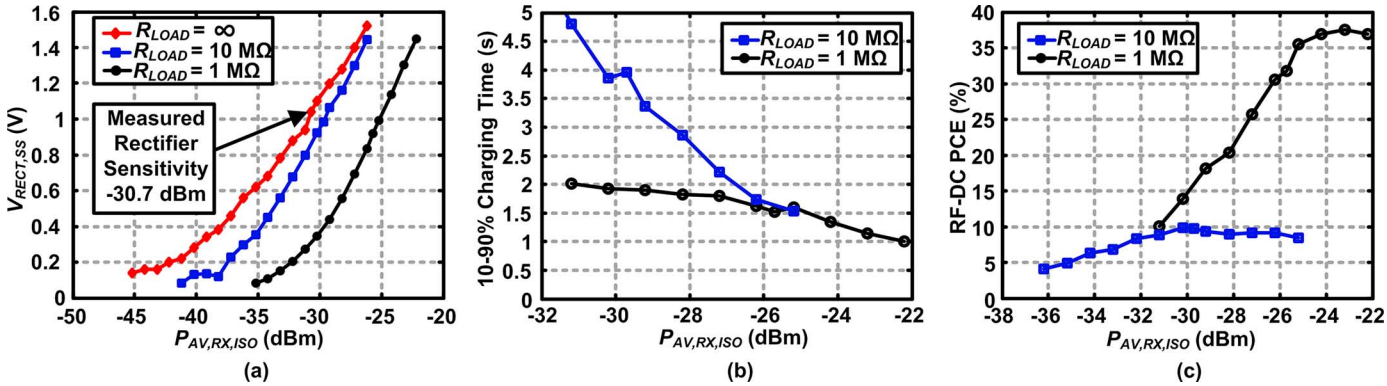

Fig. 18. Measured 2.4-GHz rectifier performance. (a) Rectifier sensitivity across target output voltage and R_{LOAD}. (b) Rectifier charging time for 1-μF storage capacitor. (c) Rectifier PCE across input power for $R_{\mathrm{LOAD}} = 1$ MΩ and 10 MΩ.

Fig. 19. Photograph of a 2.4-GHz rectifier-antenna characterization in a typical office conference room.

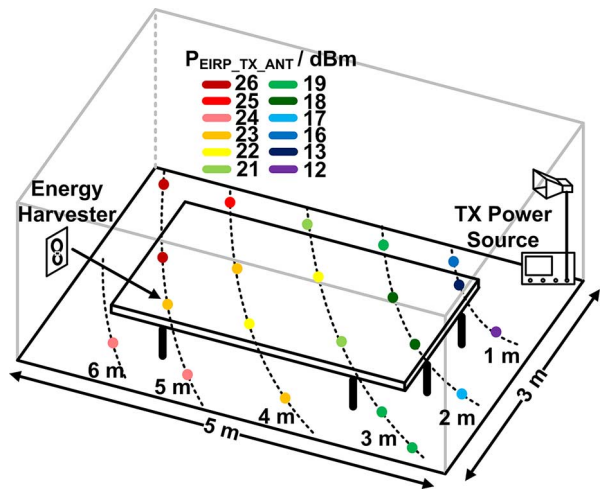

Fig. 20. Diagram of measured 2.4-GHz rectifier performance in a conference room demonstrating feasibility of wireless powering in typical office environments.

load conditions. For 1-MΩ load, the maximum PCEis 37% at $P_{\mathrm{AV,RX,ISO}}$ of -23 dBm.

The rectifier and antenna are also measured in practical scenarios. In an office corrider, 1-V $V_{\mathrm{RECT,SS}}$ can be generated with a TX EIRP of 4 W at 20-m distance, which is consistent with -30-dBm sensitivity based on (10). However, multipath fading effects and increased sensitivity to antenna orientation and position was observed. Rectifier performance is also studied in a conference room, as shown in Fig. 19. The same setup is adopted here as in the anechoic chamber, and 10-MΩ load is considered. The required TX EIRP for charging the $V_{\mathrm{RECT,SS}}$ to 1-V output is measured as shown in Fig. 20. The required EIRP gradually increases for larger separation between source and rectifier. However, the required EIRP is less than the 36-dBm FCC limit for several cases.

B. PMU and UWB TX Performance

Fig. 21(a) shows the measured bandgap output voltage across $V_{\mathrm{RECT,SS}}$. The bandgap circuit can maintain $\sim 0.48 - V$ output voltage as V_{RECT} varies from 0.5 to 1.5 V. Fig. 21(b) shows measured LDO output voltage in both charging and discharging phases. It can be seen that the PMU can switch on and off as expected and LDO can generate a constant 0.78-V supply voltage for the UWB TX block. As simulated, the PMU consumes $<$ 300nA.

The UWB TX is characterized using a connectorized 100-Ω load and with wireless measurements. Since the antenna is designed to absorb a portion of the bond wire inductance, the loading in these two cases is not equivalent. Fig. 21(c) shows the simulated and measured UWB pulse using a connectorized 100-Ω differential load. It can be seen that the measured waveform is consistent with simulations under appropriate loading conditions.

Wireless UWB TX performances is measured with TX driving an 8-GHz loop antenna shown in Fig. 15. Note that the UWB TX wireless measurements are performed using external supply for simplicity. Nevertheless, UWB pulse generation with wireless powering has been verified in measurement. In the case of the wirelessly powered UWB TX, the rectifier is loaded by the PMU in charging phase ($\sim$ 3.3 MΩ), implying a sensitivity of $\sim$ -25 dBm for the rectifier in this mode [Fig. 18(a)]. Wireless UWB signals are received using a 12-dBi gain 4–12-GHz wideband horn antenna followed by an LNA with 23-dB gain (including cable losses) driving a 25-GHz

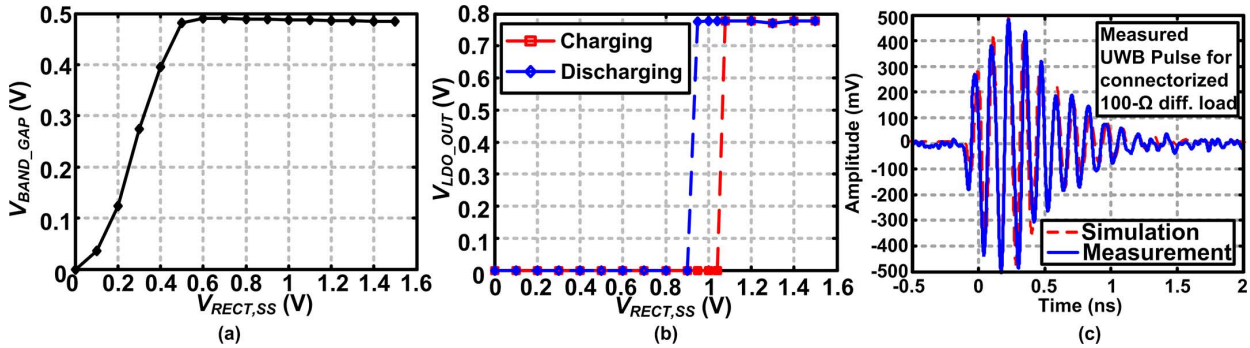

Fig. 21. Measured PMU and 8-GHz UWB TX performance. (a) Low-voltage bandgap operates with $V_{\mathrm{RECT,SS}} > 0.5$ V. (b) Measured LDO output demonstrating constant UWB TX voltage supply as well as appropriate enable/disable during charging and discharging phases. (c) Comparison of simulated and measured 8-GHz UWB pulse when UWB TX is characterized with connectorized 100-Ω differential load.

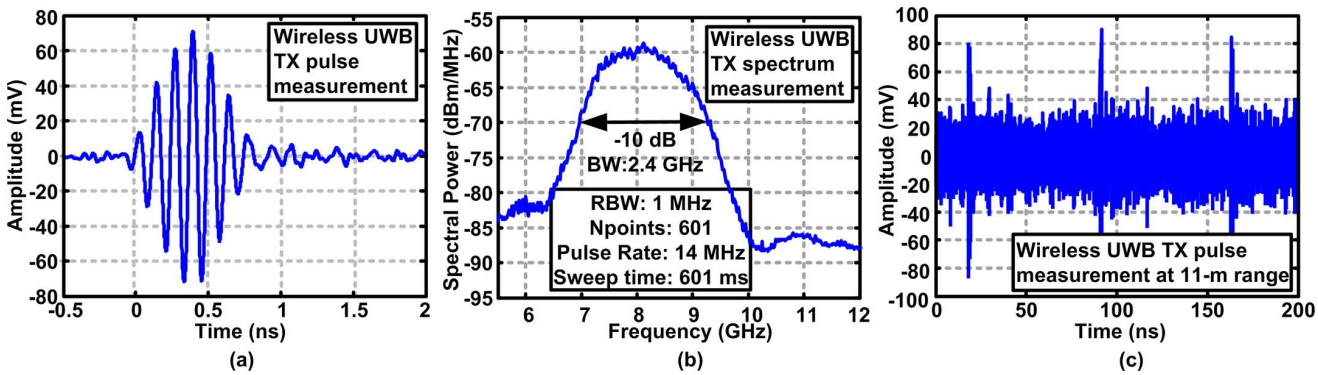

Fig. 22. Wireless measurements of UWB TX in the (a) time domain and (b) frequency domain. Measurements are consistent with 0-dBm UWB TX radiated power. (c) UWB TX pulse achieves > 15-dB SNR at 11-m range, demonstrating feasibility of operation beyond 10 m.

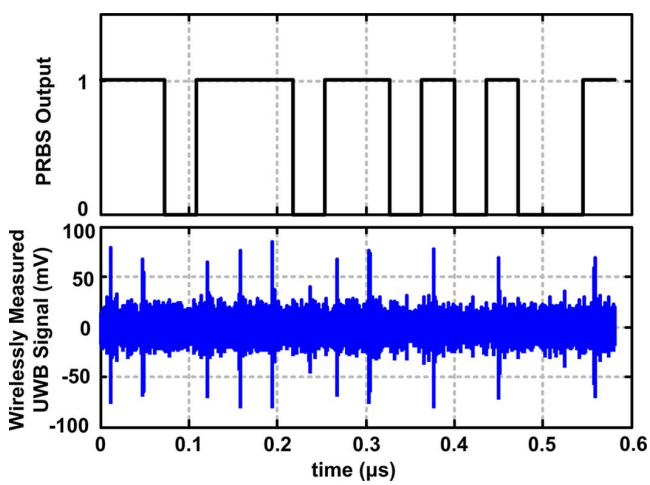

Fig. 23. Comparing output of on-chip PRBS which modulates UWB TX and wirelessly measured OOK UWB TX signal at 11-m range.

oscilloscope. Fig. 22(a) and (b) shows wireless measurement and UWB spectrum. Assuming 60-dB path loss (3 m at 8 GHz), the measured ~ -13 dBm signal is equivalent to $\sim$ 0-dBm radiated power at the loop antenna, which is consistent with the simulated 750-mV peak–peak differential output. The low pulse-repetition frequency (6–28 MHz) ensures UWB spectral FCC mask compliance. When pulses are generated at 28 MHz, the UWB transmitter consumes 64 pJ per pulse (14 mW when radiating a pulse).

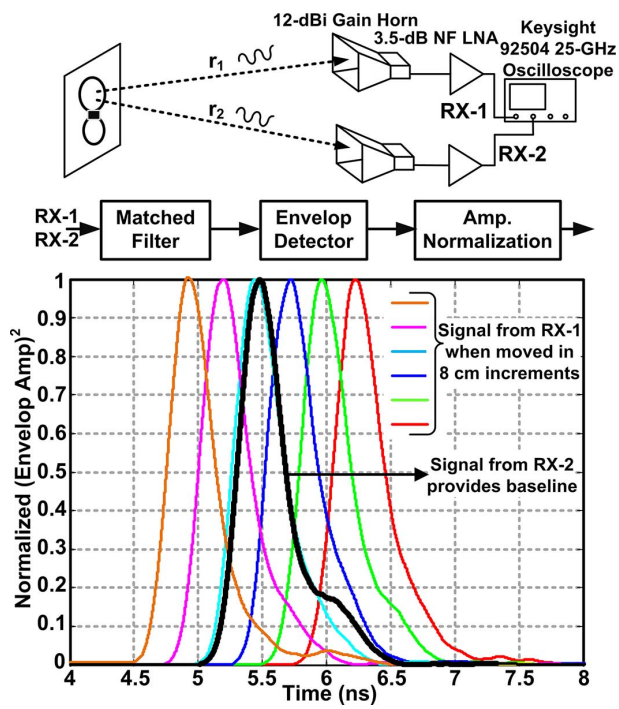

Fig. 24. Relative TOF measurement using the UWB TX. RX-2 provides baseline while the position of RX-1 is varied.

The choice of storage capacitance C_{STORE} is dictated by desired UWB payloads. Given PMU thresholds for UWB TX

TABLE II
RECTIFIER PERFORMANCE COMPARED WITH THE STATE OF THE ART

Rectifier	Technology	Antenna Area	Sensitivity	Frequency	Distance	MAX PCE	Requirement
This work	65 nm CMOS	1.33 cm^2	-30.7 dBm@1 V	2.4 GHz	20 m@4 W EIRP	37%@-23 dBm	Deep N-Well
JSSC 14 [30]	90 nm CMOS	12 cm^2	-27 dBm@1 V	868 MHz	27 m@1.78 W EIRP	40%@-17 dBm	Control Loop
JSSC 11 [33]	90 nm CMOS	No Antenna	-24 dBm@1 V	915 MHz	-	16%@-16 dBm	Deep N-Well
JSSC 08 [32]	0.25 μm CMOS	30 cm^2	-22.6 dBm@1 V	906 MHz	15 m@4 W EIRP	30%@-8 dBm	External Pre-Charge

TABLE III
UWB TX PERFORMANCE SUMMARY

UWB TX	This work	ISSCC 14 [38]	ISSCC 13 [39]	ISSCC 12 [40]	JSSC 11 [41]
Technology	65 nm CMOS	65 nm CMOS	0.18 μm CMOS	90 nm CMOS	130 nm CMOS
Frequency	6.9-9.3 GHz	7.75-8.25 GHz	9-12 GHz	6-9 GHz	7.25-8.5 GHz
V_{DD} Voltage	0.8 V	1 V	3.6 V	1 V	1.35 V
Power	1.8 mW	1 mW	22.4 μW	3.5 mW	0.93 mW*
Data Rate	28 Mb/s	1 Mb/s	0.03 Mb/s	0.85 Mb/s	5 Mb/s
Energy/bit	0.064 nJ/bit	1 nJ/bit	0.747 nJ/bit*	4.12 nJ/bit	0.186 nJ/bit
Antenna Area	1.02 cm^2	No Antenna	On-chip 2 mm Monopole	Not Shown	No Antenna
V_{pk-pk}	750 mV@Antenna	-	700 mV@50 Ω Coax Load	-	2.2 V@50 Ω Coax Load

enable, 1.1 V, and UWB TX disable, 0.9 V [Fig. 21(b)], a 1-μF capacitor implies 0.2-μJ energy is available from the capacitor in each charge–discharge cycle. At 64 pJ/pulse, this can support a payload with $\sim$ 3000 pulses.

For long-distance wireless measurement, the UWB is received using an antenna/LNA setup with $\sim$ 3.5-dB noise figure (NF). The received signal is shown in Fig. 22(c) and achieves $>$ 15-dB SNR at 11-m range (limited by test setup). The OOK modulated data is generated by an on-chip PRBS. Fig. 23 compares the PRBS output from the chip with the wirelessly measured UWB pulse sequence, demonstrating OOK-modulated UWB TX performance at range exceeding 10 m.

Localization using relative TOF triangulation is emulated using the setup shown in Fig. 24. Two identical receiving paths are used. RX-1 is moved to different locations away from the chip package while RX-2 works as a reference providing a fixed baseline in the testing. The received pulses from RX-1 and RX-2 are processed by a matched filter followed by envelop detection. For different RX-1 locations with 8-cm distance increment and TOF with RX-2 staying stationary, the normalized envelop amplitudes demonstrate sub-10-cm ranging resolution.

The performance of the rectifier and UWB TX is summarized and compared with previous state of the art in Tables II and III. The rectifier achieves 2.3 $\times$ improvement in sensitivity over the state of the art with 9 $\times$ smaller antenna area ($\sim$ 1.3 cm^2). The 8-GHz UWB TX operates from a 0.8-V supply and consumes only 64 pJ to generate each UWB pulse while achieving 2.4-GHz 10-dB bandwidth at 8 GHz.

V. CONCLUSION

A batteryless wirelessly powered UWB SoC has been demonstrated that achieves state-of-the-art rectifier sensitivity while meeting size and weight constraints. The UWB SoC design is based on a rectifier modeling and systematic optimization methodology that is generally applicable across other frequencies and rectifier applications, including wake-up receivers. Rectifier measurements in practical environments and sub-10-cm ranging using the UWB TX with a TDOA approach demonstrates feasibility of batteryless localization sensors with $\sim$ 10-m range while operating under FCC specifications. Future research efforts include further improvement of rectifier sensitivity and reduction in rectifier load currents during the charging phase. Ongoing efforts to deploy the UWB SoC for insect localization demonstrate the possibilities for miniaturized wirelessly powered positioning tags for Internet of Things applications.

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