STMicroelectronics
Deep Sub-Micron Processes

120nm, 90nm, 65 nm CMOS
Feature Size

- High density
- Low power
- More system Integration
- More Process Features

AMS 0.8µ
1.2k gates/mm²

AMS 0.6µ
3k gates/mm²

AMS 0.35µ
18k gates/mm²

ST 0.25µ
35k gates/mm²

ST 0.18µ
80k gates/mm²

ST 0.12µ
180k gates/mm²

ST 90nm
400k gates/mm²

ST 65nm
800k gates/mm²

1994 at CMP

2006 at CMP
Process Roadmap

Feature size, 1983 - 2010

- Industry (SIA where available)
- CMP

Year

Size, microns

CMP annual users meeting, 18 January 2007, PARIS
STMicroelectronics
CMOS 0.12 µ
HCMOS9
HCMOS9 Process Features

- 0.12µ mixed A/D CMOS SLP/6LM (triple Well)
- Gate length (0.13 µm drawn, 0.11 µm effective).
- 6 Cu metal layers. (Up to 8 metal layers in option)
- Low k inter-level dielectric
- Power supply: 1.2 V

- Multiple Vt transistor offering
  - (Ultra low leakage, low leakage, High speed)

- Threshold voltages (for 3 families above):
  - VTN = 570/500/380 mV, VTP = 590/480/390 mV

- Isat (for 3 families above):
  - TN @ 1.2 V : 410/535/680 uA/um; TP @ 1.2 V : 170/240/320 uA/um
0.12μ mixed A/D CMOS SLP/6LM introduced by CMP in Q4 2001

~ 140 centers received design rules, design-kits

- 4 runs + 1 special, organized in 2006

- 62 circuits (45 from France + 17 abroad)
  In 2005 60 circuits (13 from France + 47 abroad)

- 2500 Euro/mm²
  (25 samples for which 5 are packaged)
STMicroelectronics
90nm CMOS

CMOS090
CMOS090 CMOS 90nm Process Features

- 65nm poly length (90nm drawn)
- Dual Vt MOS transistors
- Dual gate oxide
- Dedicated process flavors for high performance or low power
- Dual-damascene copper for interconnect.
- 7 metal layers for interconnection
- 0.28um metallization pitch.
- Analog / RF capabilities.
- Fully compatible with e-DRAM
- Various power supplies supported: 3.3V, 2.5V, 1.8V, 1.2V, 1V
- Dual standard cell libraries (speed / density)
  (430 kgates/mm2 / 350 kgates/mm2).
- Total of > 1000 core cells
- Gate delay of 11ps (standard Vt)
- Embedded memories SRAM / ROM
90nm mixed A/D CMOS 7LM introduced by CMP in Q3 2004

~ 120 customers received design rules, design-kits

- 4 MPW runs + 1 Taxi run, organized in 2006
- 4 MPW runs scheduled in 2007
- 5000 Euro/mm²
  (25 samples for which 5 are packaged)
More Than 120 Customers Are Using The ST’s 90nm CMOS From CMP

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32 designs have been fabricated in 90nm CMOS in 2005.

From 14 customers:

**North America (7)**
- Berkeley Wireless Research Centre (BWRC, USA)
- CMC Microsystems (Canada)
- Sun Microsystems (USA)
- UCLA (USA)
- Stanford University (USA)
- Massachusetts Institute of Technology (MIT) (USA)
- Achronix Semi. LLC (USA)

**Europe (7)**
- ETH-Zurich (Switzerland)
- University of Stuttgart (Germany)
- VTT (Finland)
- INFN Pavia (Italy)
- Univ. of Oslo (Norway)
- Norwegian Univ of Science & Tech (Norway)
- University of Pisa (Italy)
56 designs (+75%) have been fabricated in 90nm CMOS in 2006.

From 16 customers:

**North America (7)**

- Berkeley Wireless Research Centre (BWRC, USA)
- UCLA (USA)
- Stanford University (USA)
- Massachusetts Institute of Technology (MIT) (USA)
- CMC Microsystems (Canada) (*)
- Georgia Institute of Technology (USA)
- University of Virginia (USA)

(*) 18 Canadian Universities

**Europe (9)**

- Technical University of Denmark (Denmark)
- ISEN / IEMN (Lille, France)
- Novelda AS (Norway)
- IMEP (Grenoble, France)
- VTT (Finland)
- Univ. of Oslo (Norway)
- University of Pisa (Italy)
- INFN Pavia (Italy)
- Instituto Microelectronica Sevilla (Spain)
STMicroelectronics
65nm CMOS
CMOS065
• 65nm poly length
• Dual or triple Vt MOS transistors
• Dual or triple gate oxide
• Dedicated process flavors for high performance or low power
• Dual-damascene copper for interconnect
• Low-k (k = 2.9) dielectric
• 7 metal layers for interconnect
• 0.20 micron metallization pitch
• Analog/RF capabilities
• Fully compatible with e-DRAM
• 800 kgates/mm²
• Various power supplies supported: 2.5V, 1.8V, 1.2V, 1V
65nm mixed A/D CMOS 7LM introduced by CMP in Q4 2006

5 customers already received design rules, design-kits
~ 20 customers under approval by ST for the NDA

• 6 MPW runs planned in 2007

• 9500 Euro/mm² (minimum area = 1mm²)
  (25 samples for which 5 are packaged)

• One design submitted for fabrication in August 2006
STMicroelectronics
SiGe 0.35μ
BICMOS6G
BiCMOS6G process specifications

- Complementary bipolar process with vertical NPN & vertical isolated PNP
- Single layer poly / 5 layers metal
- Metal 5 is thick 2.5 µ Alu (high Q inductances, power supplies)
- MIM capacitors available: 2nF/mm² and 5nF/mm²
- High resistive poly: 1 kΩ/sq
- NPN 3.3 V (Fₜ = 45 GHz,  = 0.8dB)
- NPN 5.0 V (Fₜ = 25 GHz)
- Standard Power Supplies: 3.3 V or 5.0 V
BICMOS6G
SiGe HBT transistor architecture

Schematic cross section of SiGe HBT
SEM cross sectional view of SiGe HBT
Vertical Isolated PNP structure
(Poly base emetteur)
Isolated NMOS
Applications

- High performance RF designs
  - HBT components with high Ft and low noise.
  - High Q integrated passive components (R, L, C)
- High Performance mixed A/D designs
  - HBT bipolar + CMOS : Excellent Analog environment
  - Standard digital cells libraries
- System on chip designs
  - High density CMOS digital library
  - N-ISO layer for blocks isolation (RF / Analog / Digital / …)
MPW runs

- Introduced at CMP in 2000
  ~ 50 customers received design rules and design-kits

- 950 Euro/mm$^2$
  - Minimum charge is the price of 3 mm$^2$.
  - Delivery of 25 samples for which 5 are packaged.
  - Open to every Institution or Company, (under NDA).

- 2 MPW runs scheduled in 2007.
BiCMOS7RF Technology

0.25µm SiGe:C BiCMOS process
For RF and Power Applications

Cellular Terminals Division
BiCMOS Technologies

- **BICMOS9**
  - 0.13µm CMOS
  - SiGe-C, fT/Fmax=150GHz/150GHz

- **BICMOS8X**
  - 0.18µm CMOS
  - SiGe, fT/Fmax=70GHz/90GHz

- **BICMOS7**
  - 0.25µm CMOS
  - SiGe, fT/Fmax=70GHz/90GHz

- **BICMOS6G**
  - 0.35µm CMOS
  - SiGe, fT/Fmax=45GHz/60GHz

- **BICMOS6/6M**
  - 0.35µm CMOS
  - Si, fT/Fmax=25GHz/40GHz

- **BICMOS7RF**
  - 0.25µm CMOS
  - SiGe-C, fT/Fmax=60GHz/90GHz
The next technology for RF applications (after BiCMOS6G)

An optimization of BiCMOS7 to address RF needs, BiCMOS7 being more dedicated to optical networks market (f >5Ghz).

Compared to BiCMOS6G, BiCMOS7RF:
- Have better HF noise figure
- Reduced substrate coupling
- Has power amplifier integration
- Offer high performance passive devices
- Increase CMOS density
General Features 1/3

- **CMOS**
  - Use of **HCMOS7** as the base process
  - **5 nm** gate oxide
  - **0.25 µm** gate length
  - **Shallow trench** isolation
  - Gate type N+ and P+
  - **Silicidation of gates and junctions** for low access resistance
  - Supply voltage **2.5V (2.7V max)**

- **50 Ohm.cm SUBSTRATE**
General Features 2/3

• **BIPOLAR**
  – **SiGe:C** epitaxial base (non-selective)
  – **Deep trench** isolation
  – **Quasi self aligned** structure
  – **Low-voltage HBT** (\(F_t=55\text{GHz}\) typ – \(BVCEO=2.8\text{V min}\))
  – **High-voltage HBT** (\(F_t=30\text{GHz}\) typ – \(BVCEO=6.0\text{V typ}\))
  – **Low Noise** Characteristics (\(N_{fmin}=0.4\text{dB at 2GHz}\))

• **OTHER DEVICES**
  – Polysilicon resistors: P & N type (85 & 180 Ohm/sq)
  – N+ Active resistor (60 Ohm/sq)
  – Poly/N+ sinker capacitor (2.88fF/\(\mu\text{m}^2\))
General Features 3/3

• OPTIONS
  – **HV NLDEMONS** (2.5V – BVDS=13.5V min – WxRon=3W.mm typ)
  – High value poly resistor (1kW/sq)
  – Isolated N-channel MOS
  – **Isolated Vertical PNP** (Ft=6GHz typ – BVCEO=9.5V typ)
  – 5fF/µm² MIM capacitor
  – Precise TaN resistor (35W/sq; +/-10%)

• BACK END
  – 5 metal levels / **thick top metal 2.5µm**
  – M1 in Tungsten; M2 – M5 in Aluminium
  – M5 in **thick copper 4µm** (option)
  – Bumping
## BiCMOS7RF Devices List

### MOSFETs
- 2.5V N&P MOSFETs
- Drift N&P MOS transistors
- Isolated NMOS transistor (option)
- HV NLDEMOS transistor (option)
- LV NLDEMOS transistor (option)
- LV PLDEMOS transistor (option)

### Bipolar Transistors
- Low-voltage SiGe:C NPN HBT
- High-voltage SiGe:C NPN HBT
- Isolated vertical PNP BJT (option)
- Lateral PNP transistor

### Resistors
- Silicided N+ Poly
- Unsilicided N+ Active
- Unsilicided N+ Poly
- Unsilicided P+ Poly
- Nwell under STI
- Hipo (option)
- Precise TaN (option)

### Capacitors
- 5fF/µm² MIM capacitor (option)
- N+ Poly/NWell capacitor
- N+ Poly/N+ Sinker capacitor

### Junction Diodes
- N+/Pwell
- P+/Nwell

### Varactors
- P+/Nwell diode
- P+/Nwell diode with differential structure
- MOS transistor

### Thick Metal Inductors
- Single-ended inductors
- Symmetrical and differential inductors
### Process Masks

- **Core Process (2.5V CMOS, HBTs)**: 29 masks
- **PA Bipolar Cell**: free
- **HV NLDEMOS option**: 2 masks
- **IVPNP BJT option**: 2 masks
- **Isolated NMOS option**: 1 mask (free if IVPNP)
- **High Value Poly Resistor (hipo) option**: 1 mask
- **5fF/µm² MIM Capacitor option**: 1 mask

**Future Option**
- **Precise TaN Resistor**: 1 mask
- **LV NLDEMOS option**: 2 masks (1 if HV NLDEMOS)
- **LV PLDEMOS option**: 2 masks
1500 Euro/mm²

- Minimum charge is the price of 3 mm².
- Delivery of 25 samples for which 5 are packaged.
- Open to every Institution or Company, (under NDA).

4 MPW runs expected in 2007.
STMicroelectronics
MPW Results 2006
MPW Results 2006

11 MPWs, 1 taxi, 1 special, 123 circuits, 578 mm²

- HCMOS9GP: 4 MPWs + 1 special, 62 circ., 286 mm²
- CMOS090: 4 MPWs + 1 taxi LP, 56 circuits, 257 mm²
- CMOS065: 1 MPW, 1 circuit, 2 mm²
- BiCMOS7RF: 2 MPWs, 4 circuits, 33 mm²
STMicroelectronics Runs Histogram

- CMOS065
- CMOS090
- HCMOS9GP
- HCMOS8D
- BiCMOS6G
- BiCMOS7RF

Legend:
- 2004
- 2005
- 2006

Data from STMicroelectronics.
MPW Results 2006

Industry: 28  
Research: 84  
Education: 11

France only  Europe  N. Am.  Asia

Industry  Research  Education
Conclusion

- HCMOS9 and CMOS090 expanding fastly.
- CMOS065, already in use and with a very fast expansion.
- BICMOS7RF in use and expansion.

- Excellent Partnership CMP / STMicroelectronics

- Efficient Technical Support (CMP Engineer part-time at ST)

- Still Eagerly Waiting for a SOI process from ST.