1. This is known as a scan-DFF. It is a very useful circuit since it can pass digital information from two places: from a stored register, or from a previous scan-DFF (so that you can read out the scan-DFEs if they are daisy-chained).

2. Draw the schematic (transistor form) of the complete design. Assume the multiplexer is made up of pass-gates and inverters. Assume the D-FF is as similar as possible to the HW #3 except you can simplify the CLOCK buffering aspect.

b. Size correctly the entire design. Assume everything is normalized to NMOS = 4/2.2, and PMOS = 8/2.2.
C. Sketch a complete layout of the design. Use pencil to draw the wires for the

Wizard layout. Label each node with its node name so it is easier to grade.
What is the worst case clock-to-Q delay? Assume for simplicity: \( R_p, R_n, C_{in}, C_{out}, C_{diff}, C_{inv}, C_{invout} \)

\[
\tau = (R_p + R_n) (C_{out} + C_{invout} + C_{inv} + C_{diff}) + 3 (C_{out} + C_{invout} + C_{inv} + C_{diff}) + 3 (C_{out} + C_{invout} + C_{inv} + C_{diff})
\]

**Note:** This is worst case. Some pins of Integrator need to charge the output so the delay is doubled.

\[
e_b = 0.69, R_n
\]

**Best Case:**

\[
e_b = 0.69, R_n
\]