(a) For minimum clock period you have to consider the maximum delays through each component. So, from point $X$ to $C$ the maximum delay is:

$$T_{range} + T_{delay} + T_{L} = (A + A + 2) \text{ ns}$$

$$= 2.8 \text{ ns}$$

Now your signal should propagate and reach node $C$ before $2'$ edge of $\bar{\phi}$ goes high.

$$2.8 \text{ ns} \leq 0.6 \text{ (skew)} + T/2$$

$$\Rightarrow T \geq 2.2 \times 2$$

$$\Rightarrow T \geq 4.4 \text{ ns}$$

So, minimum time period is $4.4 \text{ ns}$. 
(b) This is similar to part (a) except signal should propagate through second pass gate and inverter and logic \( l_2 \) before \( c \) goes to high. Also here skew is negative.

\[
\text{Total Delay} \leq T_{l_2} - 0.6
\]
\[
\Rightarrow 0.4 \times 2 + T_{l_2} \leq 2.5 - 0.6
\]
\[
\Rightarrow T_{l_2} \leq 1.1 \text{ ns}
\]

So, maximum allowed delay through \( l_2 \) is 1.1 ns.

\[\text{blue 3}\]

(A)

\[\text{Delay} \propto \frac{R \times C}{2} = \frac{RC}{4}\]

\[\therefore \quad \text{Delay} \leq 2X\]

i.e. more than 2X faster.

(b)

\( R \) remains same

\[C_{\text{parallel}} = \frac{C}{2} < 2X\]

\( C_{\text{finge}} \) remains same.

(c)

\( R \Rightarrow R/2\)

\( C_{\text{finge}} \) increases slightly slightly < 2X
(a) \[ R = \frac{8L}{\omega T} \Rightarrow R \Rightarrow 2R \]
\[ C \Rightarrow C/2 \]
So, \( RC \Rightarrow RC \) \( \leq 2x \)

(b) \[ R \Rightarrow R \]
\[ C \Rightarrow C/4 \]
\( > 2x \)

(c) \[ P \times v^2 \]
Power reduced to 1/4.

(g) Propagation delay of line doesn't depend on voltage.