1. For the circuit shown below, find:
   a. $V_{in}$ at the input to the 75Ω T-line
   b. $V_{junct}$ and $V_{time}$ at the node "junct" using SPICE
   c. Write the netlist for the circuit, simulate and confirm your calculations.

   ![Circuit Diagram](image)

   Please use the node names given above.

2. Consider the circuit below:

   ![Circuit Diagram](image)

   You have been assigned this "problem" circuit to fix. The PCB with this circuit has already been fabricated and 250 malfunctioning boards are on hold on the manufacturing floor.

   Excessive overshoot and undershoot are causing the 74ACT04 to die prematurely. Your job is to fix the boards with a minimum of "newwork". You may not change the driver or receiver chips. The 33Ω resistor is changeable. The nodes "junct" and "time-output" are accessible.

   Your solution must prevent the ESD diodes from turning on in the 74ACT04. Also, transitions at its inputs must be monotonic and must maintain proper $V_{IH}$ and $V_{IL}$ levels. See 74ACT04 data sheet for the specs.

   (25) Show your solution schematic, netlist & proof in simulation.

   (10) Explain your solution.
3. You are using a 74HCT4 to drive a low impedance T-line. The \( I_{ON}/V_{OH} \) and \( I_{OL}/V_{OL} \) curves for the output stage are shown below. Of the six inverters in the package, four are available for you to use. The receiver being used is also a 74HCT4. Both driver and receiver are operating at 5V. Be sure to meet \( V_{OH} + V_{IL} \) at the receiver for incident wave switching. Limit overshoot/undershoot to less than 10% of \( V_{CC} \). Use expected minimum curves @ 25°C.

Show your final schematic, netlist & simulation results. Be sure to label all signals & component values. Assume \( t_{r} = t_{f} = 2ns \) for the 74HCT4 outputs.

\[ \text{Input model:} \]

\[ \begin{aligned}
\text{Available inverters:} & \quad \begin{array}{c}
\text{input model:}
\end{array} \\
& \quad \begin{array}{c}
\text{1.2mF} \\
5pF \\
10mF
\end{array}
\end{aligned} \]

\[ \begin{aligned}
\text{n-channel sink capability} & \quad \text{p-channel source capability} \\
\text{75 points total}
\end{aligned} \]