

Sample-and-Holds

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Sample-and-Hold Circuits

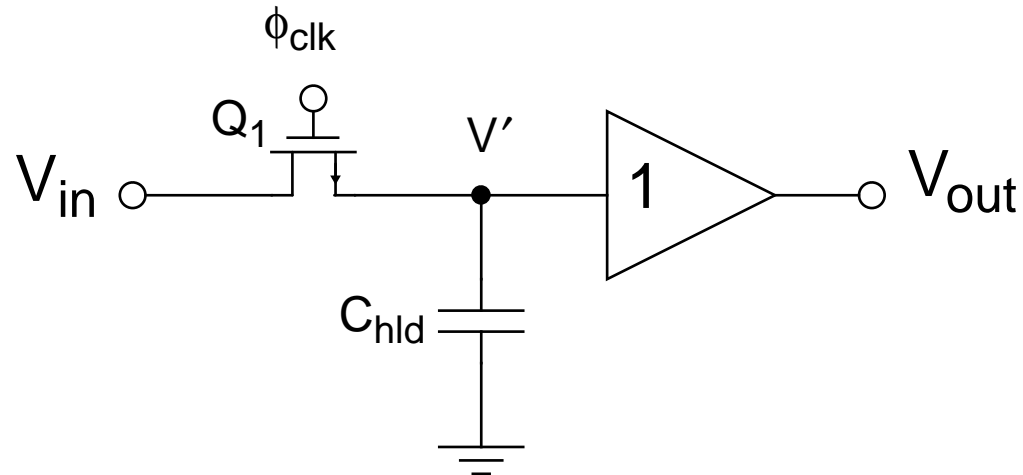
- Also called “track-and-hold” circuits
- Often needed in A/D converters
 - Conversion may required held signal
 - Also reduces errors due to different delay times

Errors in Sample-and-Holds

- ***Sampling pedestal or Hold Step***
 - errors in going from track to hold
 - should be signal independent for no distortion
- ***Signal feedthrough*** — should be small during hold
- ***Speed*** — due to bandwidth and slew-rate limitations
- ***Droop rate*** — slow change during hold mode
- ***Aperture (or sampling) jitter*** — effective sampling time error in time; difficult in high-speed designs



Basic Concept



- Basic circuit has some practical problems

Charge Injection

- Causes hold step

Aperture Jitter

- Sampling time variation function of V_{in}



Charge Injection

- When ϕ_{clk} goes low, channel charge on Q_1 causes V' to have negative step.
- If clock edge fast, 1/2 flows each way.
- Channel charge

$$\Delta Q_{C_{hld}} = \frac{Q_{CH}}{2} = \frac{C_{ox}WL V_{eff-1}}{2} \quad (1)$$

$$V_{eff-1} = V_{GS1} - V_{tn} = V_{DD} - V_{tn} - V_{in} \quad (2)$$

resulting in

$$\Delta V' = \frac{\Delta Q_{C-hld}}{C_{hld}} = -\frac{C_{ox}WL(V_{DD} - V_{tn} - V_{in})}{2C_{hld}} \quad (3)$$



Charge Injection

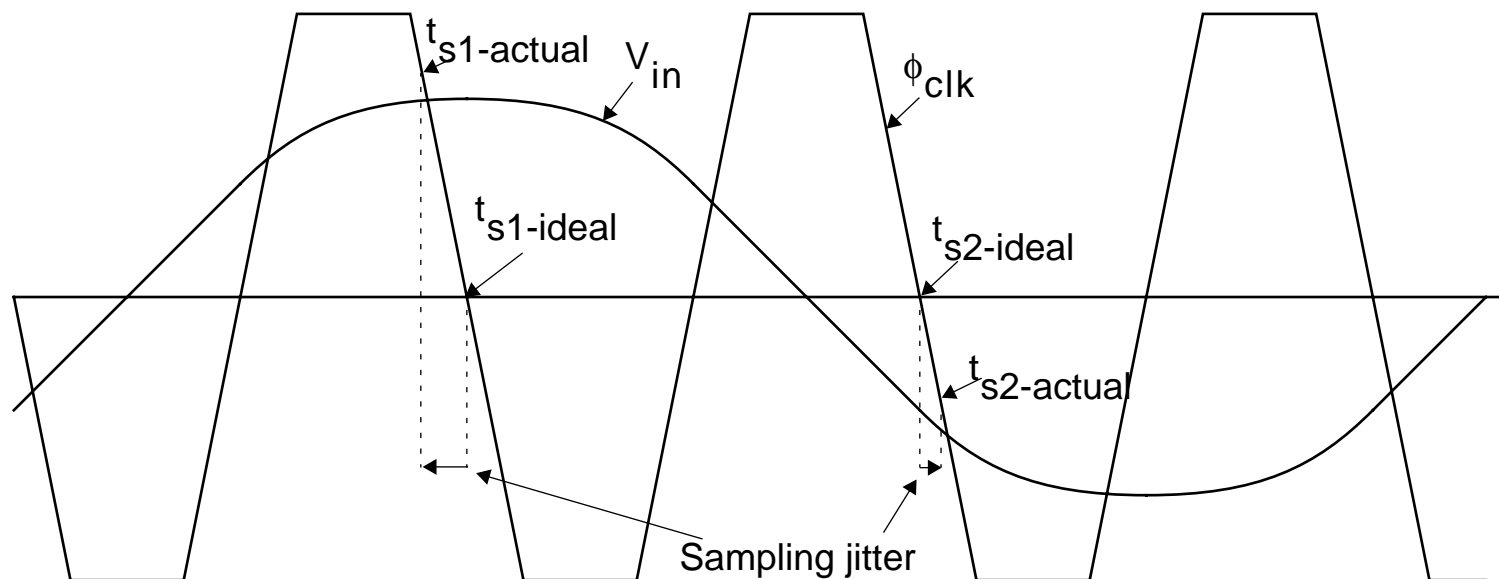
- $\Delta V'$ linearly related to V_{in} — **gain error**
- $\Delta V'$ also linearly related to V_{tn} , which is nonlinearly related to V_{in} — **distortion error**
- Often gain error can be tolerated but not distortion
- Also change due to the overlap capacitances

$$\Delta V' \cong - \frac{C_{ox} W L_{ov} (V_{DD} - V_{SS})}{C_{hld}} \quad (4)$$

- Causes dc offset effect



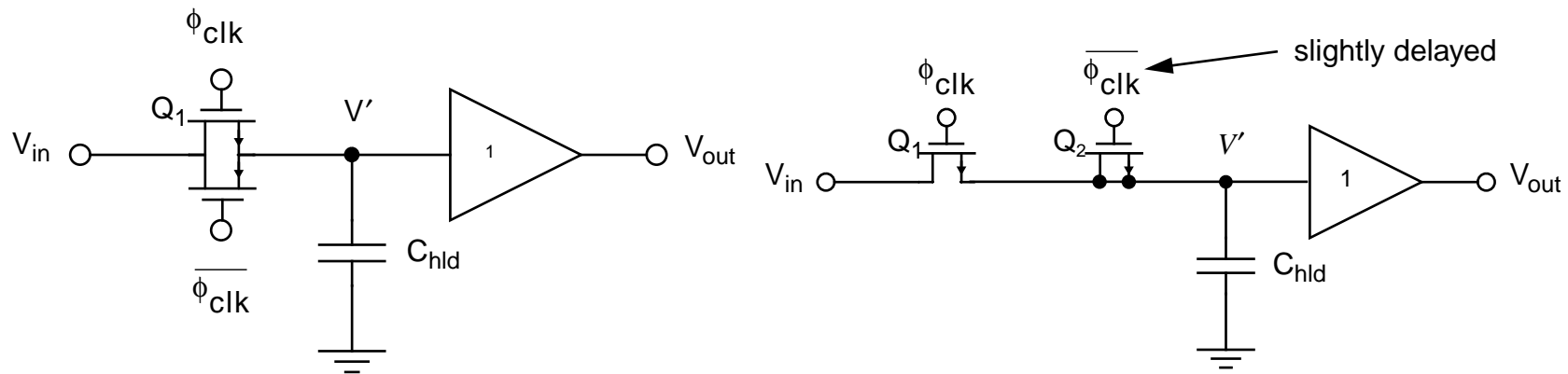
Aperature Jitter



- Q1 turns off when clock falls to within V_{tn} of V_{in}
- True sampling time depends on value of V_{in} — ***distortion***



S/H Charge Reduction



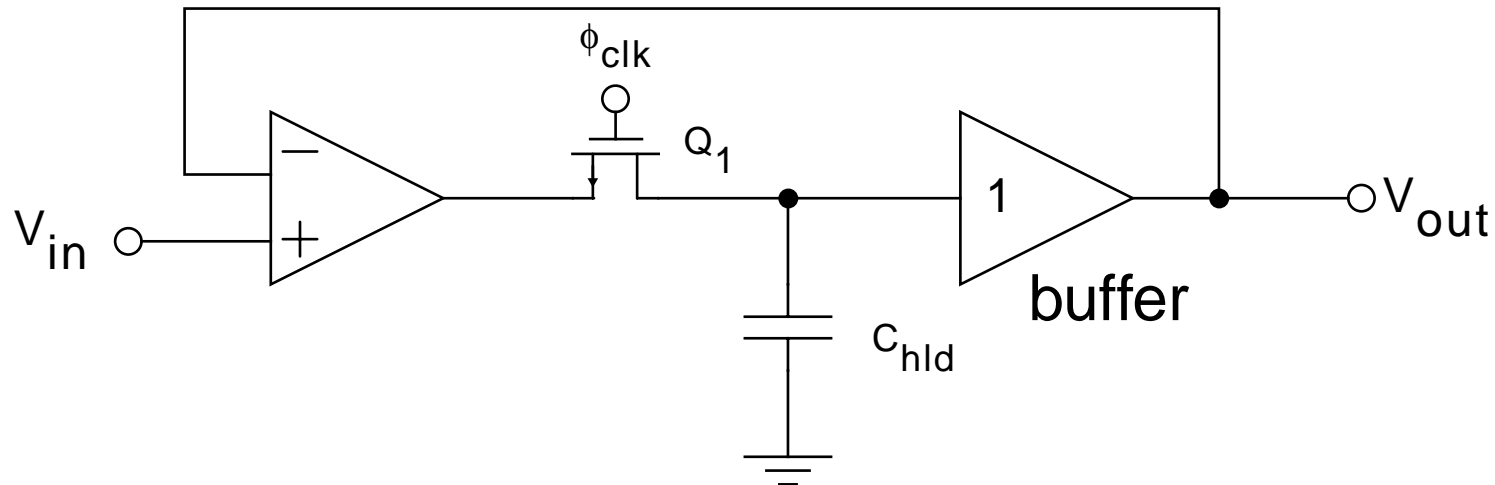
CMOS transmission gate

Dummy switch

- Transmission gate — difficult to make p and n transistors match
- Dummy switch
 - Q_2 is 1/2 size of Q_1 to match charge injection
 - difficult to make clocks fast enough so exactly 1/2 charge is injected
 - up to 5 times better than without dummy



High Input Impedance



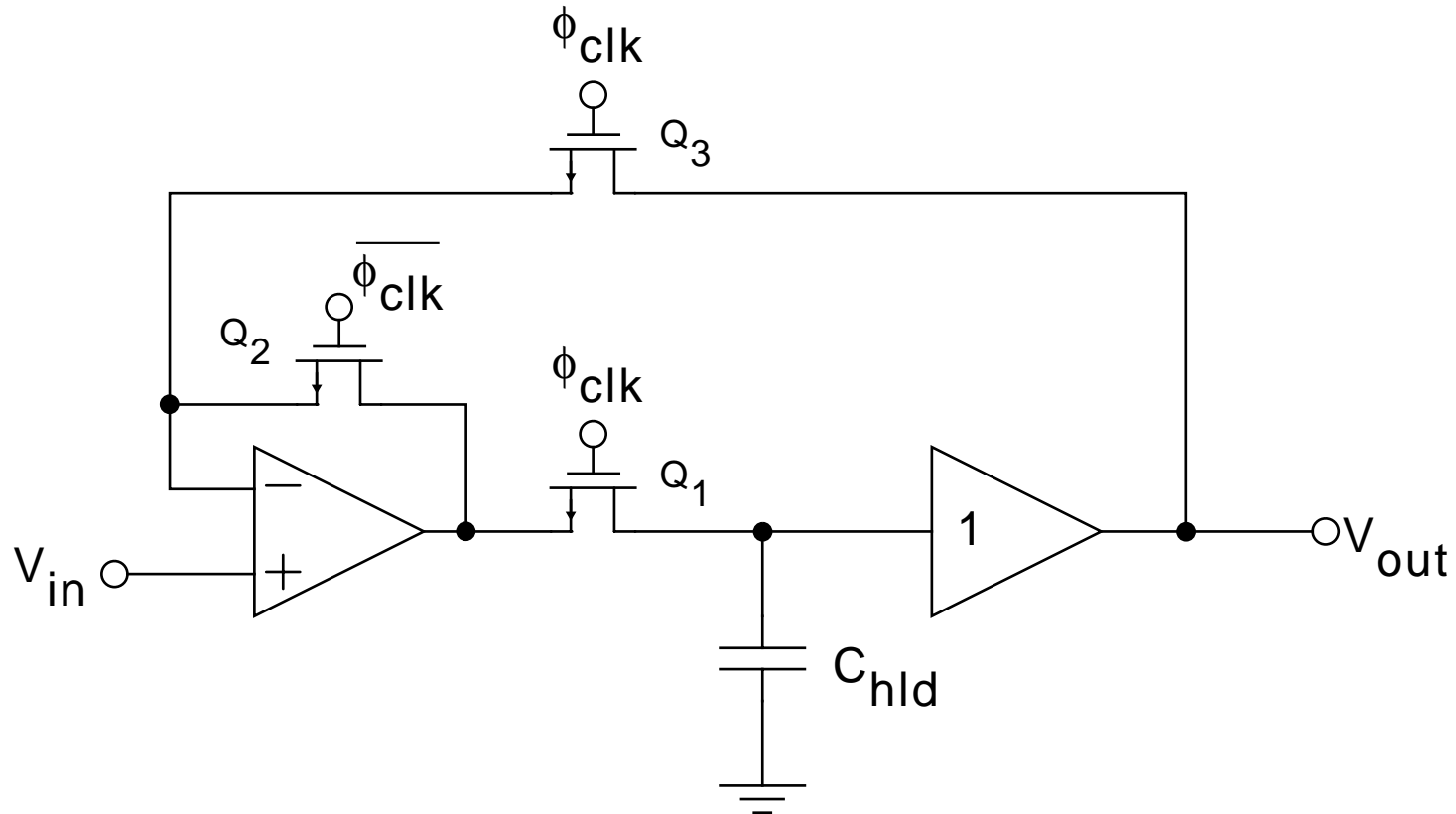
- dc offset of buffer divided by loop gain

Disadvantages

- Opamp output must have fast slew rate
- Samp time, charge inject — input signal dependent
- Speed reduced due to overall feedback



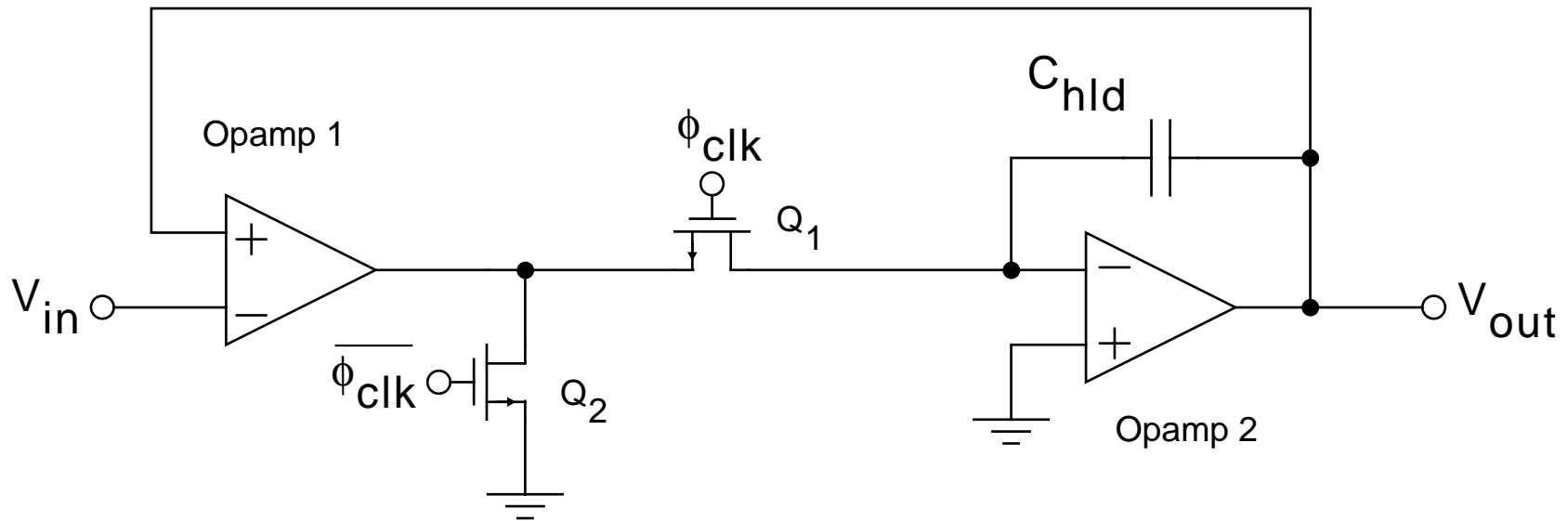
Reduced Slew Rate Requirement



- Samp time, charge injection - input signal dependent



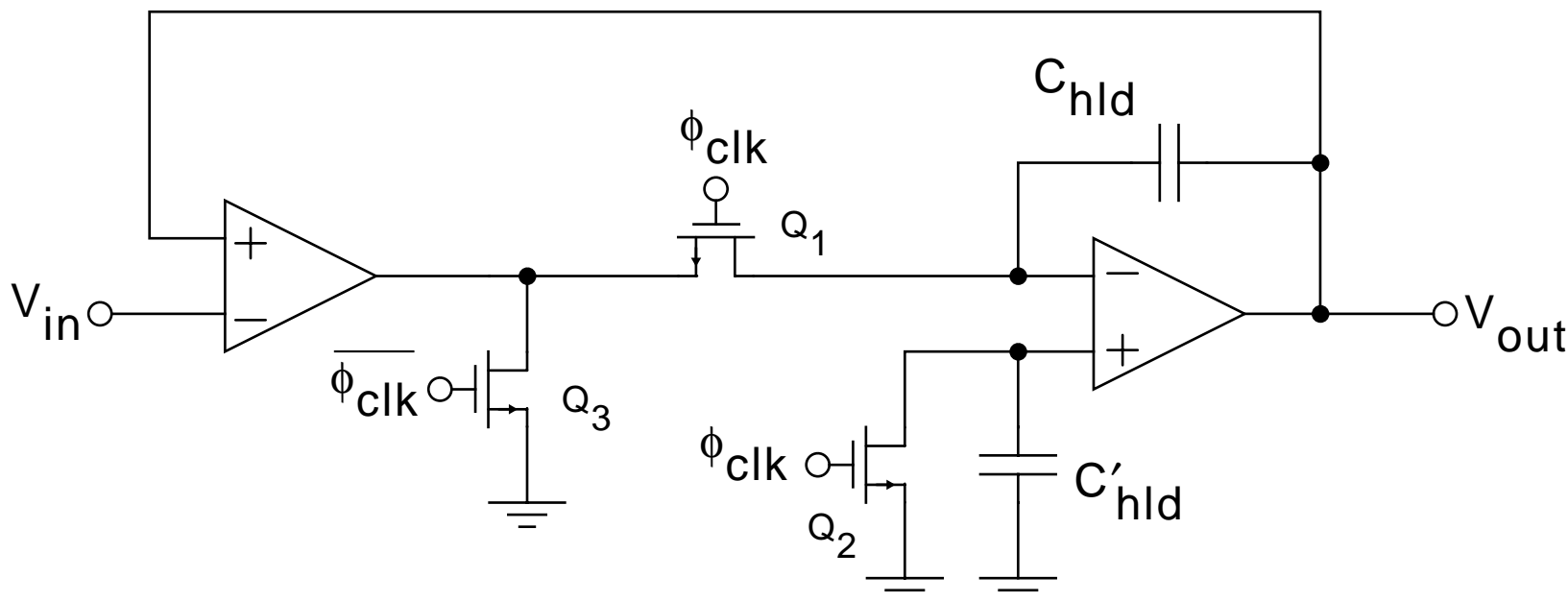
Input Signal Independence



- Q1 always at virtual ground
- Samp time, charge injection - NOT dependent
- Charge injection causes ONLY dc offset
- Q2 used to clamp opamp1 output near ground
- **Slower** due to two opamps in feedback



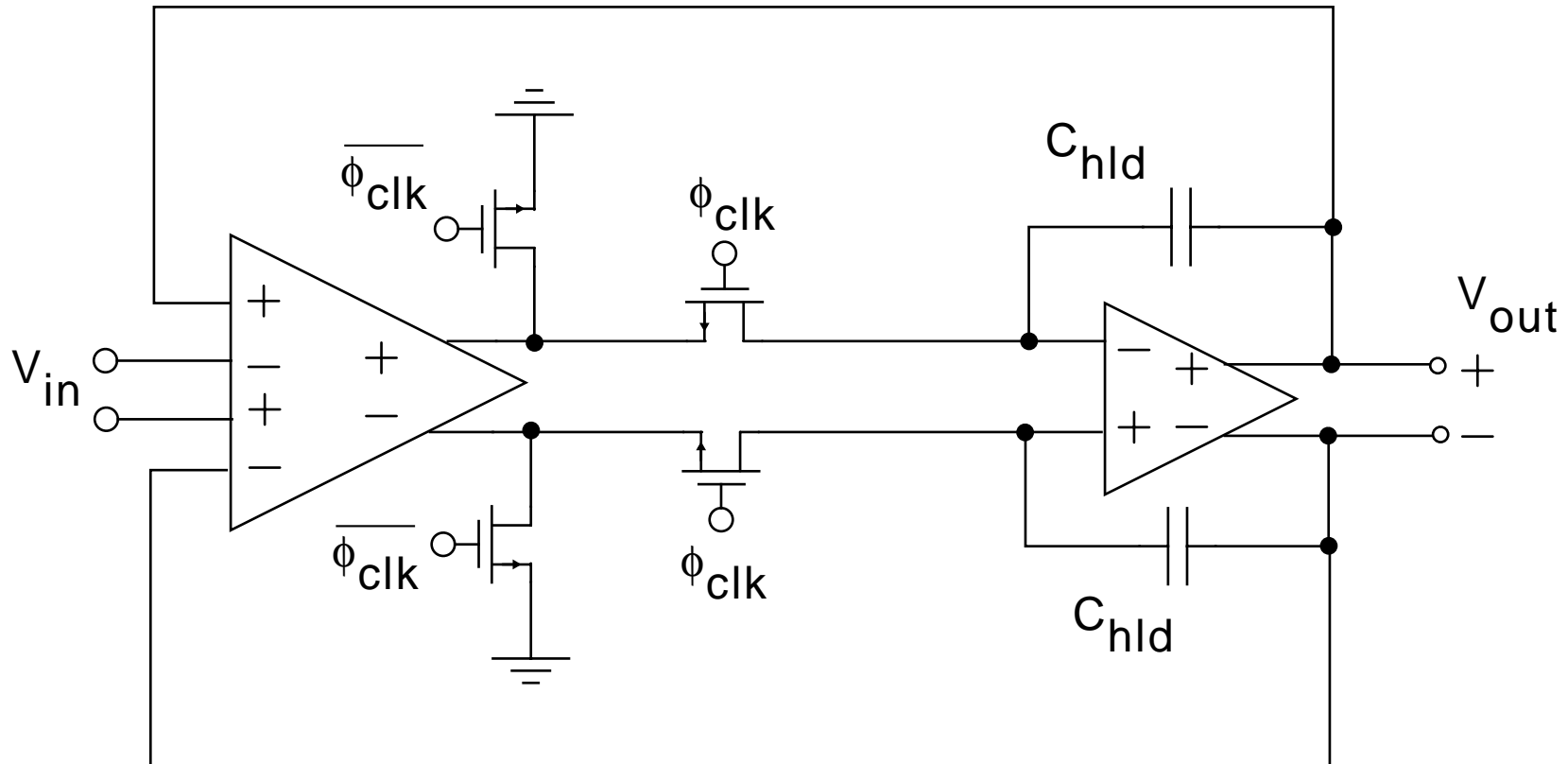
Reduced Offset (Single Ended)



- Charge injected by Q_1 matched by Q_2 into C'_{hld}
- If fully differential design, matching occurs naturally leading to lower offset.



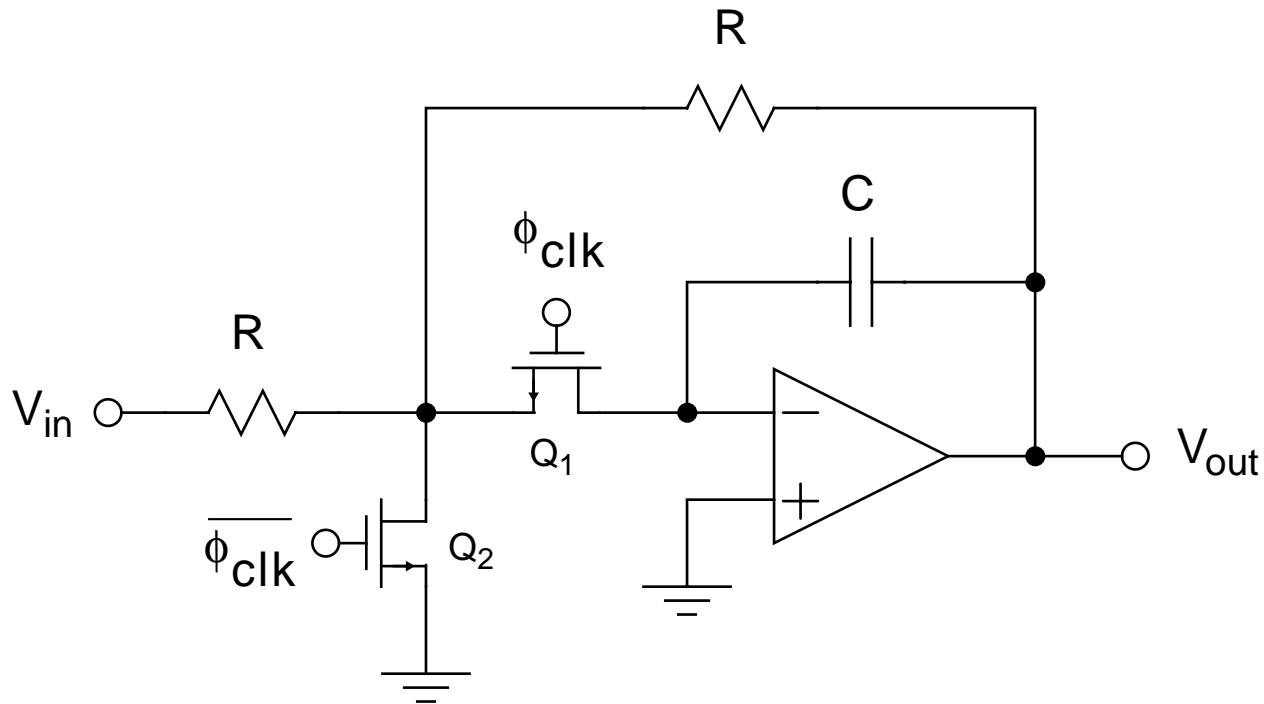
Reduced Offset (Differential)



- Gnd is common mode voltage



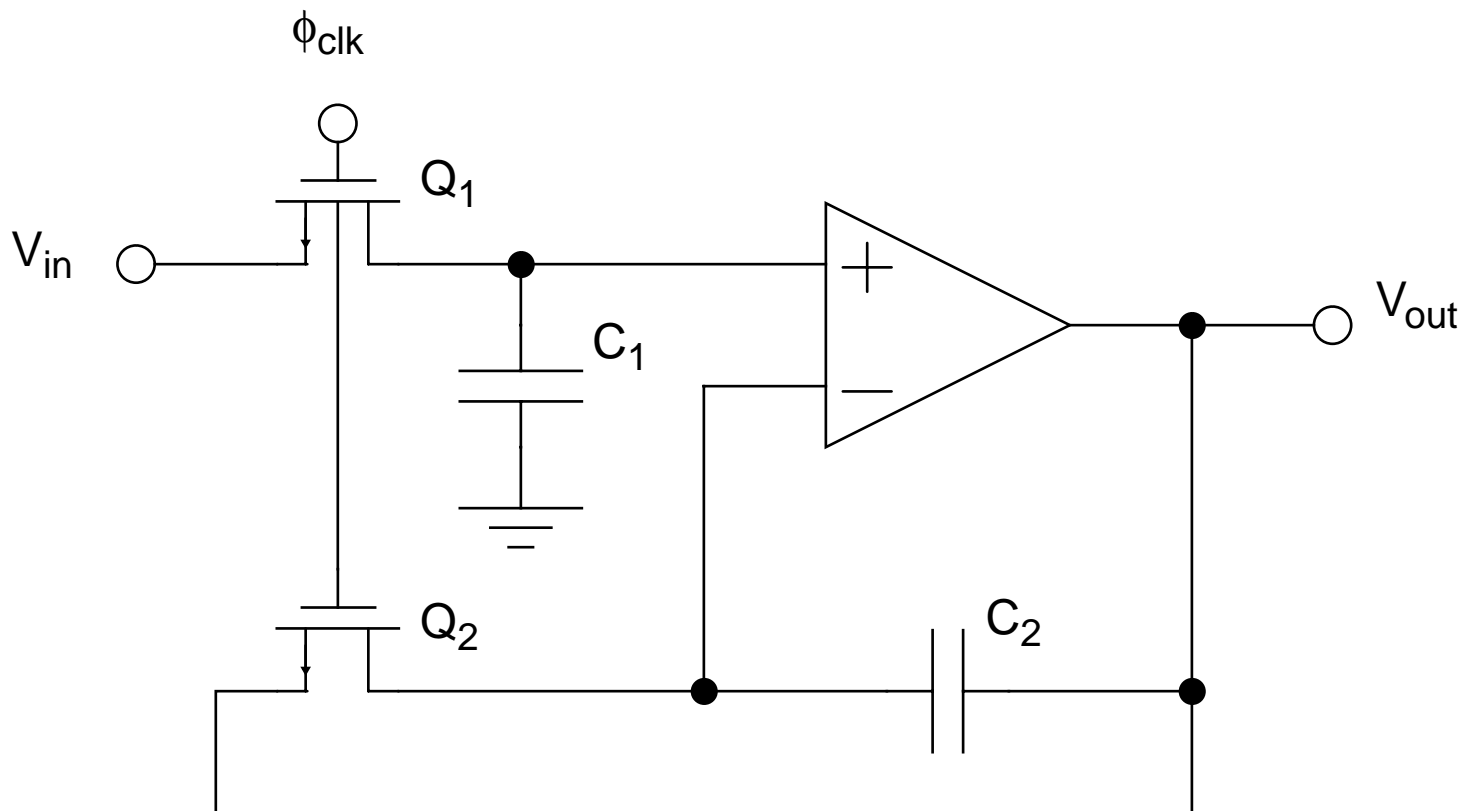
Example #1 (BiCMOS)



- Needs opamp capable of driving resistive loads
- Good high-speed BiCMOS configuration
- $\omega_{-3 \text{ dB}} = 1/(RC)$ when in track mode
- Might add a small input capacitor



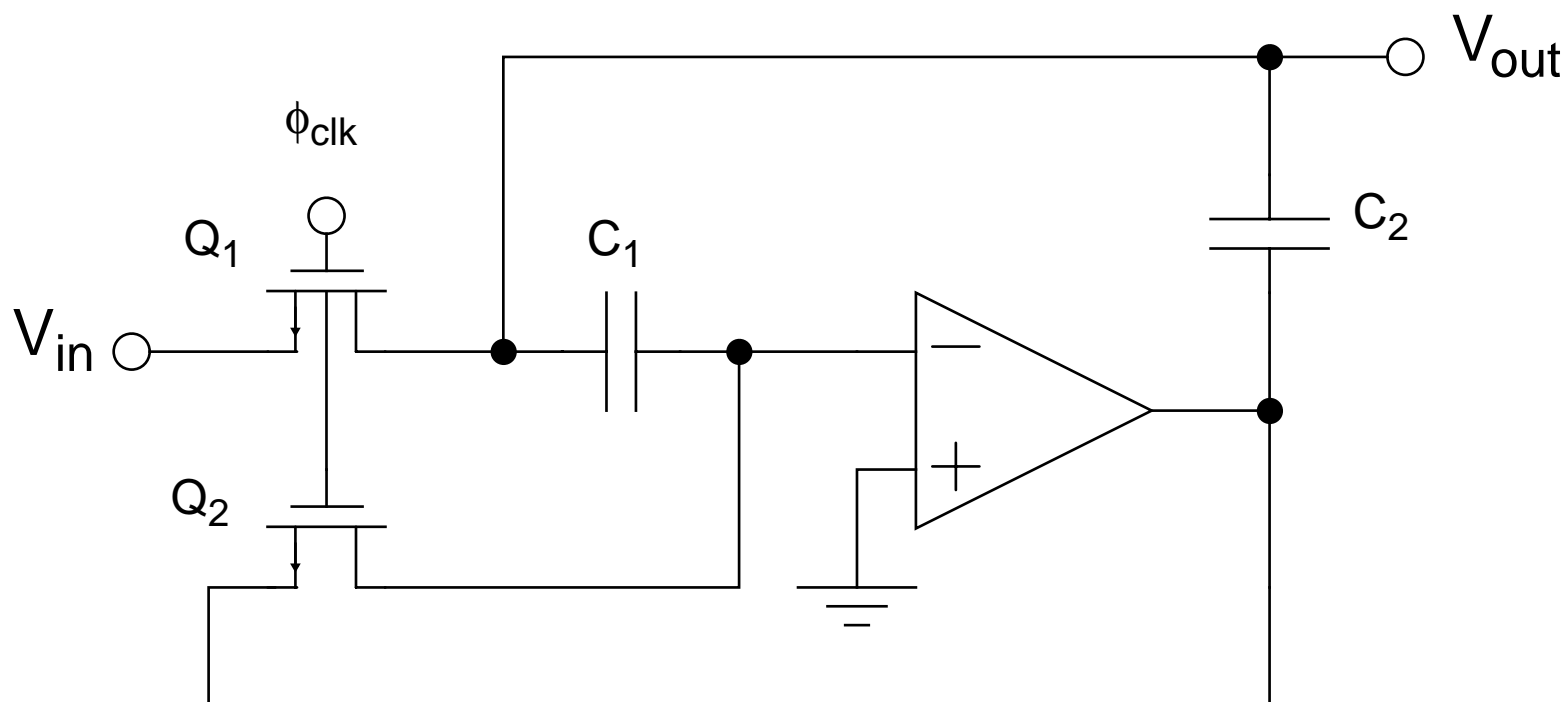
Example #2



- Charge injection of transistors cancel
- Clock signals are signal dependent
- Good speed, moderate accuracy



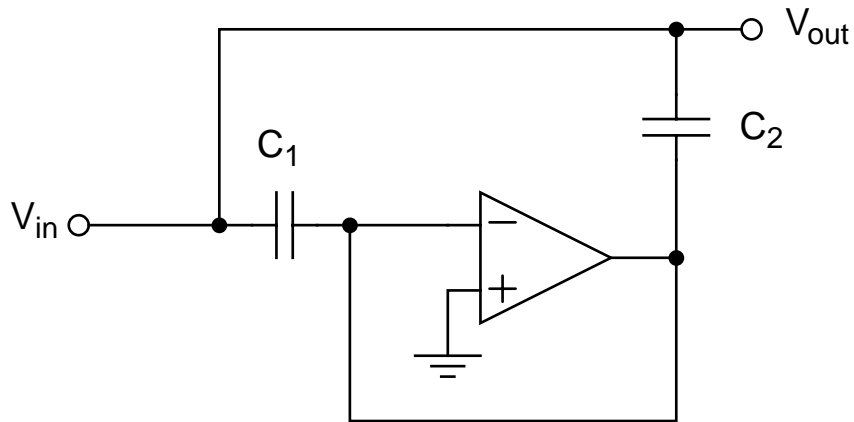
Example #3



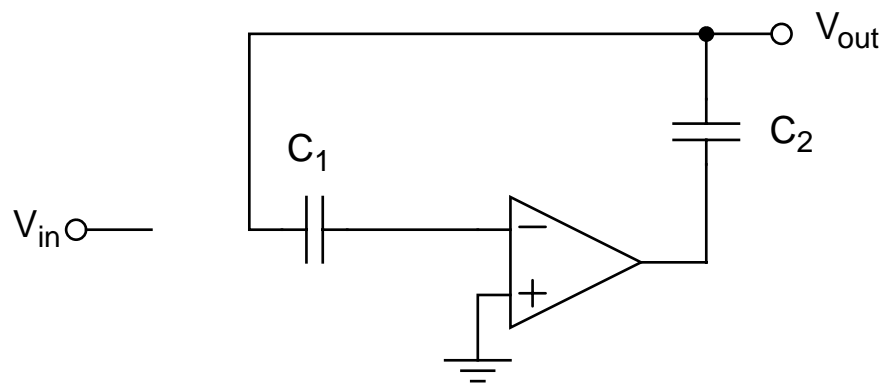
- Hold capacitor is large Miller capacitor
- Can use smaller capacitors and switches — good speed
- If Q_2 turned off first, injection of Q_1 small due to Miller effect



Example #3 (cont'd)



Sample Mode



Hold Mode

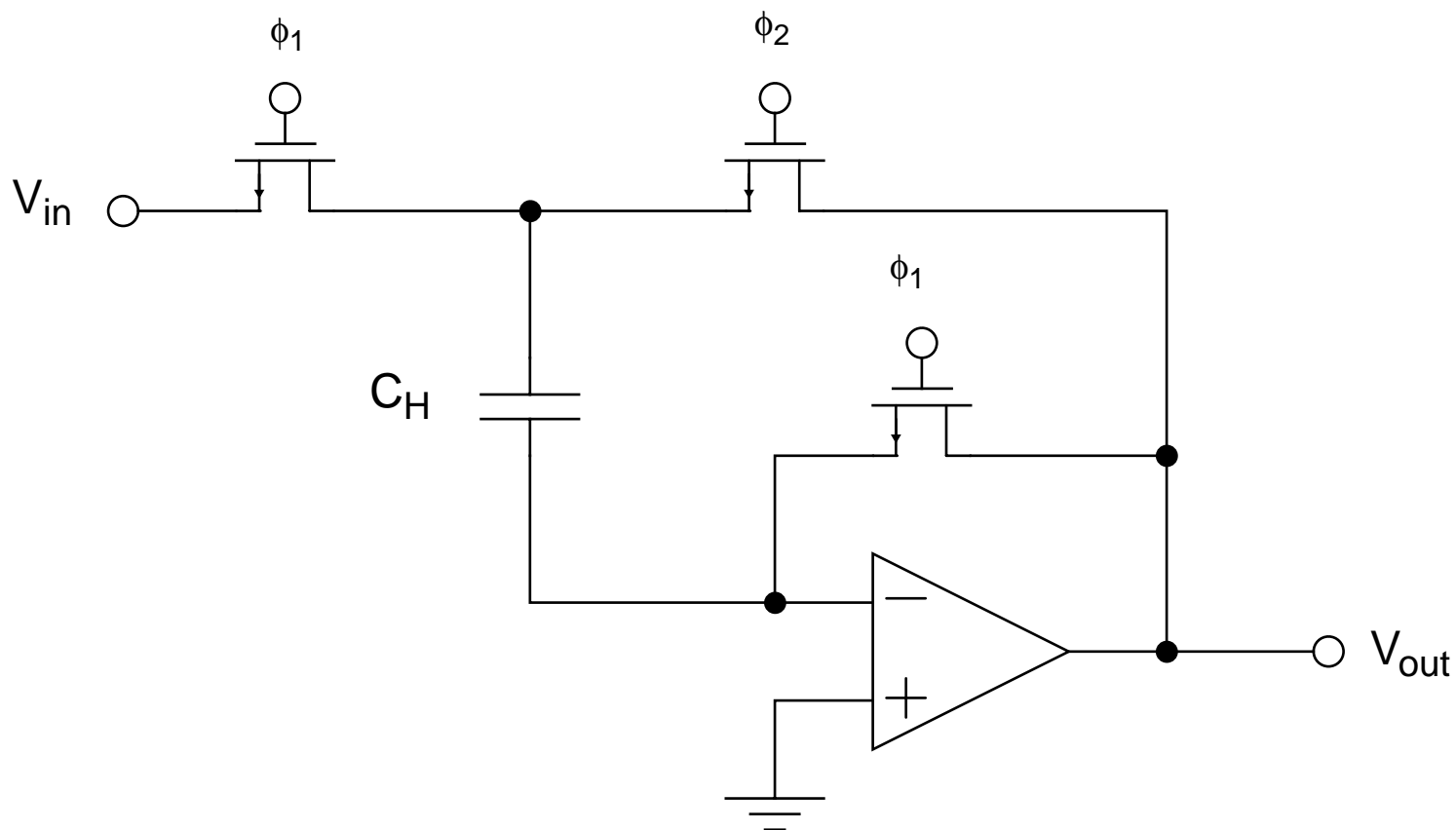
- Miller cap

$$(1 + A) \left(\frac{C_1 C_2}{C_1 + C_2} \right)$$

- Amp output does not swing much
- Higher speed amplifier possible



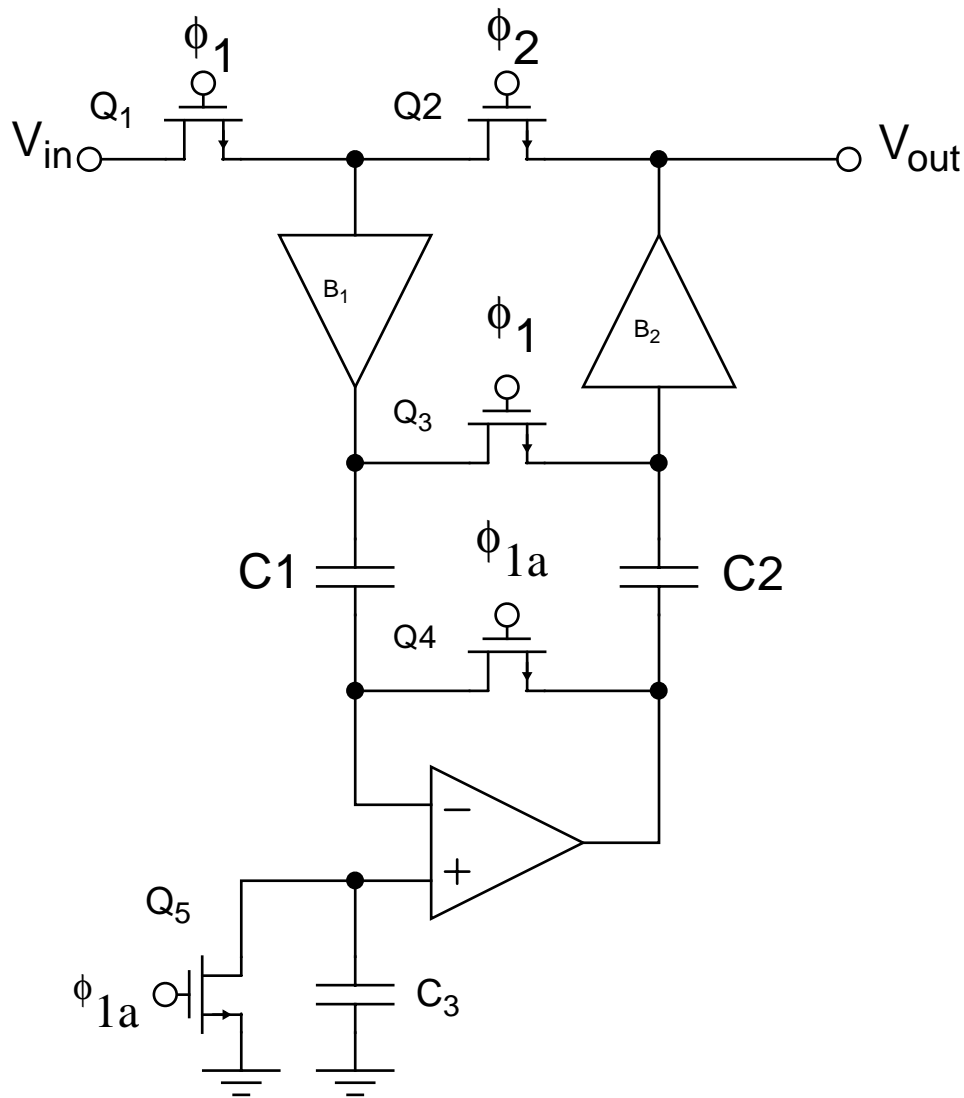
Example #4



- Accurate since offset cancellation performed
- Slow since opamp swings from 0 to V_{in} every cycle



Example #5



- Improved accuracy
- High input imped
- ϕ_{1a} -> advanced
- Charge inj of Q_4 and Q_5 cancel (and is signal indep)
- Charge inj of Q_1 and Q_2 - no effect
- Charge inj of Q_3 reduced as before

